

**GD** CONTROL DATA  
CORPORATION

96750629

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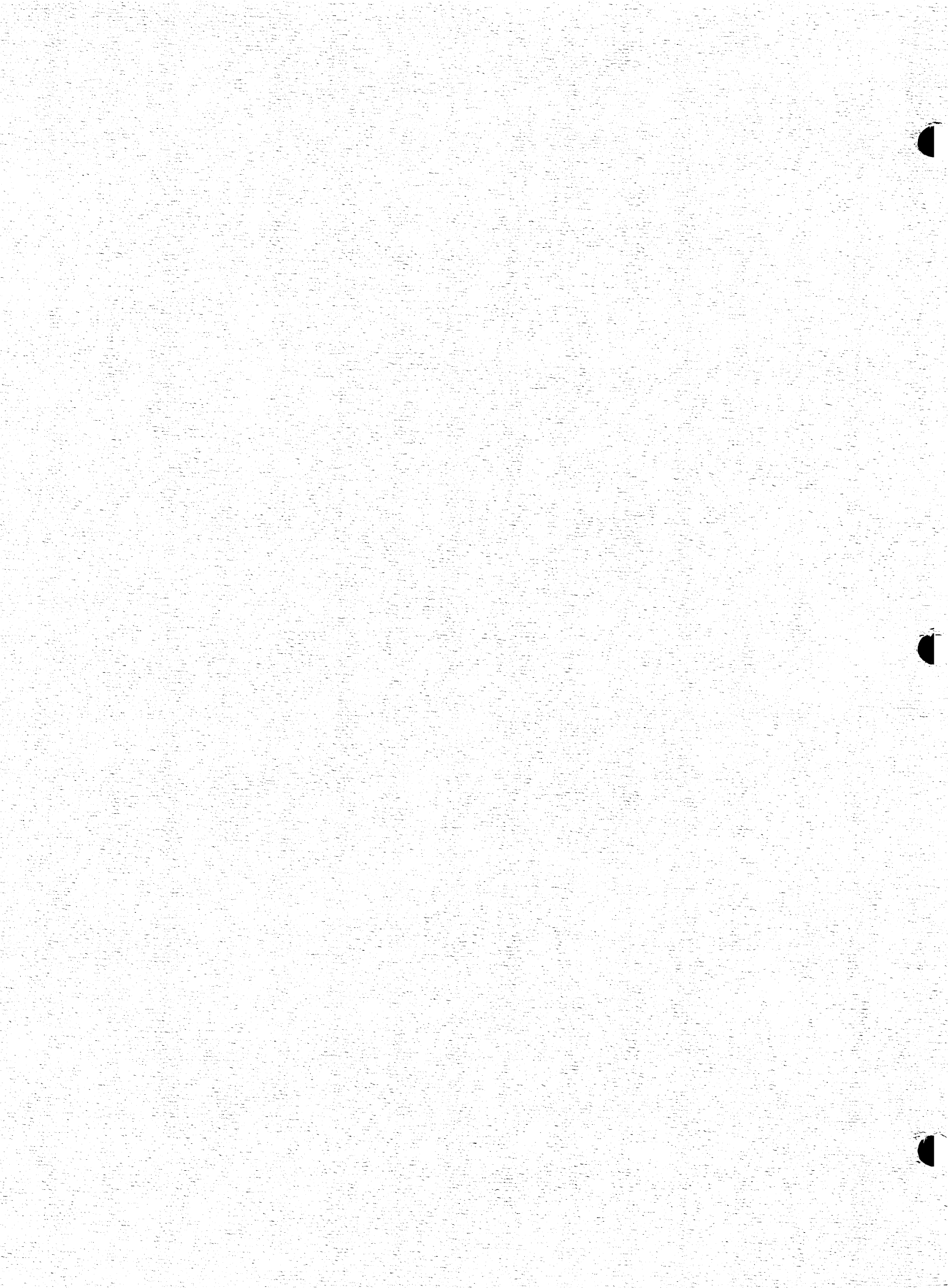
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**CDC®**  
**SERIAL I/O UNIT**  
**DK611-A**

GENERAL DESCRIPTION  
OPERATION  
INSTALLATION AND CHECKOUT  
THEORY OF OPERATION  
DIAGRAMS  
MAINTENANCE  
PARTS DATA

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**HARDWARE REFERENCE/MAINTENANCE MANUAL**



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**HARDWARE REFERENCE/MAINTENANCE MANUAL**



## PREFACE

This manual describes the DK611-A equipment which is mounted in a 1750-1/2 Computer Interface Unit. A GD128-A, +15 Volt Power Supply, is needed for each 1750 module to power the DK611-A units. One GD128-A can provide power for up to 15 DK611-A equipments.

Additional information may be found in the following publications:

<u>Description</u>	<u>Publication Number</u>
1700 Computer Reference Manual	60153100
1700 Computer System Manual	60152900
Introduction to Data Communications	13798900
1500 Product Family Index	88980000
1750-1/2 Computer Interface Unit	88980100
Key to Logic Symbols Manual	88981500
Data Communications	RS232-C Specification

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## Section One

### GENERAL DESCRIPTION

#### 1.1

#### GENERAL

The serial I/O card (hereafter called the SIO) provides a flexible communications interface between the computer and serial data (RS232-C or 20ma current loop) compatible devices such as cathode ray tube (CRT) terminals, printers, etc. Its primary functions are to convert serial data from the communications line to parallel format for input to a computer and to convert parallel data received from the computer for serial output to the communications line.

The SIO consists of two functional sections, send and receive, which are composed of data handling and control. The send section accepts various function commands from the computer which are used in the data transfer process. The receive section provides necessary interface and control circuits to transfer the status of the modem or communications facility to the computer via the CIU/CIE. The send and receive controls are contained on a 40 pin Universal Asynchronous Receiver Transmitter (UART) integrated circuit.

The SIO card features include:

- A crystal-controlled clock - 0.01% overall stability
- Selectable baud rates - 50 to 19,200
- RS232-C Compatible option
- Current loop/photodiode send/receive option for high common mode voltage environments
- Selectable send/receive word lengths - Five, six, seven, or eight data bits
- Send and receive parity select - Odd, even, or no parity

- Modem control for full duplex operations - RS232-C Standard interface type A through E
- Selectable detect of character (EOT)- Detecting end of buffer data block, specific character, etc.
- Selectable Transmit inhibit by Clear to Send (RS232) or an external restraint signal (current loop)

Interface cable connection from a terminal device to a SIO card is made by connector insertion over the CIU/CIE backplane. (See Figure 1.1 for a typical system configuration.)

1.2

### PHYSICAL DESCRIPTION

The SIO card occupies one unit location of the CIU/CIE module which has a total single module capability of 15 SIO cards. The SIO card uses the read status capability (Q bit 7=1), and therefore cannot use station 0 of the CIU/CIE module. (See the Computer Interface Unit/Computer Interface Expander Manual, Section 2.3.4). The SIO card dimensions are 7-3/4 x 9 inches.

1.3

### ELECTRICAL DESCRIPTION

The SIO card requires +5 vdc power, supplied by the CIU/CIE module, plus a +15 vdc power supply which is a standard supplement to the CIU/CIE module power. One +15 vdc power supply is adequate for up to 15 SIO cards. The logic elements used on the SIO card are primarily transistor-transistor logic (TTL). The TTL voltage levels are:

Logical one = +2.4v to +5.0v

Logical zero = 0 to +0.4v

The interface to terminals and modems are +12 volt signals per the RS232 specification.

The current loop drive levels for the photodiode detection option are:

Logical one = 20 ma (Marking)

Logical zero = 0 to 0.1 ma (Space)

Logic levels can be reversed (Mark = no current ) by adding a jumper.

Refer to Section Three for details.

## 1.4 PERFORMANCE/CHARACTERISTICS SUMMARY

### 1.4.1 PERFORMANCE

The following paragraphs outline the performance characteristics of the SIO unit.

#### 1.4.1.1 Baud Rates

The SIO contains a crystal-controlled dual (separate Send/Receive) baud rate generator which provides 16 rates of 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200 baud. Send and Receive have a separate set of four Dual Inline Package (DIP ) switches to select one of the 16 rates. See Table 2.4 for the switch settings vs output baud rate.

#### 1.4.1.2 Line Driving Capability

Terminals up to 50 feet away may be wired directly to the SIO with the RS232 convention provided the ground common mode voltage is 2V or less. Data transceivers (modems) would be required if the RS232-C terminal is greater than 50 feet away or high common mode voltages exist. The optically isolated option is used with current loop (nominal 20ma) in a high common mode voltage environment. Unipolar voltage current loop operation at rates to 9600 baud over 1000 ft of cable are possible. Bipolar operation is available for longer cable lengths.

#### 1.4.1.3 Error Detection

Parity, line break, and lost character errors are detected and available for interrupt and status.

#### 1.4.1.4 Modem Capability

Full or half duplex modem communications control, excluding auto answer, disconnect, auto dialing and secondary channel operation is available.

#### 1.4.1.5 Data Word Lengths

Word lengths of five, six, seven, or eight data bits may be selected by DIP switches on the board.

#### 1.4.1.6 Parity

Odd, even or no parity may be selected by DIP switches on the board.

#### 1.4.1.7 Inhibit Transmit

Clear-to-Send (RS232-C) or an external current loop signal (Restraint) may be selected by soldered wire jumpers to inhibit the request for new Transmit data.

#### 1.4.2 RELIABILITY

The mean time between failures (MTBF) is 75,000 hours.

#### 1.4.3 MAINTAINABILITY

The mean time to repair (MTTR) is 0.5 hours (card replacement).

#### 1.5 EQUIPMENT CONFIGURATION

The SIO card connects into one unit location of the computer interface unit. One interface cable per card is required to interface to a terminal device or modem. Terminal devices will require interface cables assembled per the system requirement.

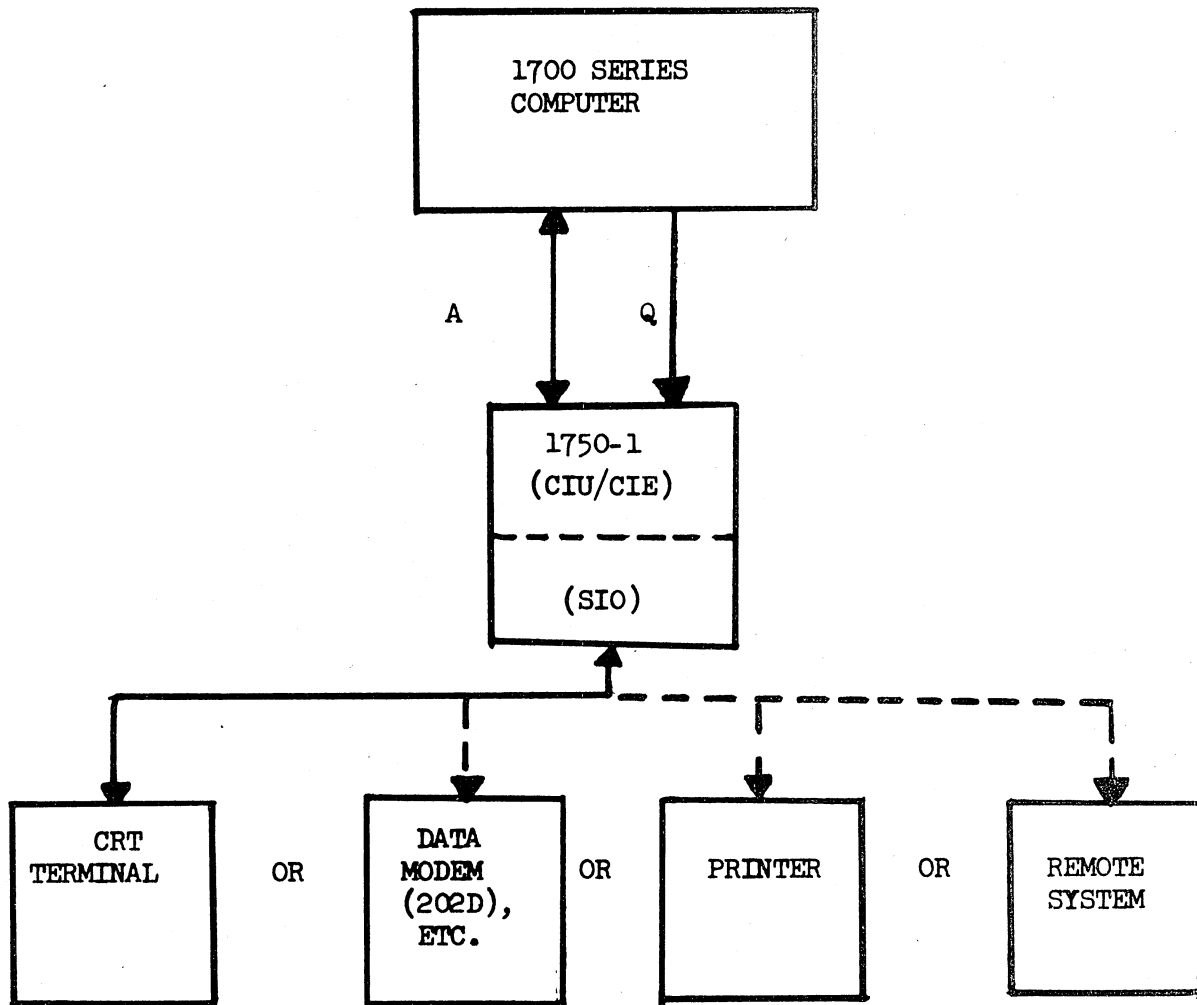


Figure 1.1 Typical System Configuration

## Section Two

### OPERATION

#### 2.1

#### CONTROLS

The Serial I/O card has several modes of operation. A specific mode will be selected for a system application by pre-setting a number of miniature DIP switches and wire jumpers. Miniature (DIP) switches are used to select the send or receive baud rates, word lengths, parity mode, stop bit (s) and the EOT character. Individual wire jumpers on the board select operation of the external current loop Restraint signal. The mode of operation (RS232 or current-loop) is selected by a set of pre-wired jumpers and components on a 28-pin adapter plug that mates with an integrated circuit socket.

#### 2.1.1

#### Miniature Switches

There are three miniature switch modules, S1 - S3, which are used to set word lengths for the UART (S3), set the send data rate and/or receive data rate (S2) and select a character for the special character detection (EOT detect) circuitry on receive (S1). Tables 2.1 through 2.4 list the functions selectable by S1-S3.

Table 2.1 Transmit and Receive Word Length Select

S3 switch		Word Length
3	2	
Off	Off	8 bits
Off	On	7 bits
On	Off	6 bits
On	On	5 bits

Word length is the number of bits in the data word. Start, stop, and parity are additional bits. These switches set the word length for both send and receive.

→ shell spec.

Table 2.2. Parity Select

S3 Position		Parity Condition
1	5	
X	Off	No parity bits
Off	On	Even Parity
On	On	Odd

No parity means no send bit generated and no receive parity checked. Even or odd means the total number of logic ones in the word length and the parity bit (inclusive) is either odd or even.

x= don't care.

*L2 shell spec*

Table 2.3 Stop Bit (s) Select

S3-Position 4	Stop Bit (s)
On	One
Off	Two (1.5 special)

If the word length selected by S3-2 and-3 is 5 bits and the switch S4 is off, one and a half (1.5) stop bits will be sent and checked on receive.

### Special Character (EOT) Select

S1 switches 1-8 set the special character detect character. The switch is programmed so if a one is desired, the switch position is off. A zero requires the switch be set to the on position. Any word select (00-FF) 16 may be configured. The numbers above the switch correspond to the bit position. For example, detecting a ~~6B~~ would require a data bit setting of 01101011 for bits 07 thru 00 so 7, 4 and 2 would be on and 6, 5, 3, 1 and 0 would be off. Note that if less than eight bits is programmed with switches 2 and 3 of S3 the word will be right justified - i.e., bit 00 will contain the least significant bit and the unused bit (s) will be zeros (low). For the shorter word lengths, the unused bit switch(es) must be on. For example, to detect a special 6 bit word, bit positions 07 and 06 must be on.

Table 2.4 Send (Receive) Baud Rate Select

S2 is divided in two groups of 4 switches. Switches 1-4 are used to select one of 16 possible baud rates for the send circuitry while switches 5-8 select a separate one of 16 baud rates for the receive circuitry.

S2 Switch				Transmit (Receive) Baud Rate
1 (5)	2 (6)	3 (7)	4 (8)	
on	on	on	on	50
on	on	on	off	75
on	on	off	on	110
on	on	off	off	134.5
on	off	on	on	150
on	off	on	off	300
on	off	off	on	600
on	off	off	off	1200
off	on	on	on	1800
off	on	on	off	2000
off	on	off	on	2400
off	on	off	off	3600
off	off	on	on	4800
off	off	on	off	7200
off	off	off	on	9600 ✓
off	off	off	off	19,200

NOTE: Extreme care should be taken when using current-mode at 19,200 baud. Long line cable length resistance and capacitance can cause transition times to approach the 52µsec period.

2.2

Wire Jumpers

Wire jumpers are used to connect the options selected when using the current-mode restraint. A wire jumper between E 13 and E 14 is necessary to enable the restraint input to the inhibit transmit gate. The other jumpers are used to condition the receive circuit for loop power supply-SIO or the external send circuit provided.

Table 2.5 Restraint Receive Jumpers

Jumpers	Condition
E 9 to E 11 E 10 to E 12	SIO supplies +12v loop power
E 9 to E 12	External circuit supplies power

If the external circuit supplies power, the limiting resistor, R15, may need to be changed. See Appendix A for examples and calculations.

2.3 Jumper Module

Selection of RS-232-C or the various types of current mode is programmed by insertion of a pre-wired jumper plug into the 28 pin socket at E 8. Several types of jumper plugs are described in Appendix A.

CAUTION: Extreme care must be taken when changing jumper plugs. Particular attention should be paid to making certain not to reverse the jumper module. With certain jumper configurations this could short the  $\pm 12v$  to ground.

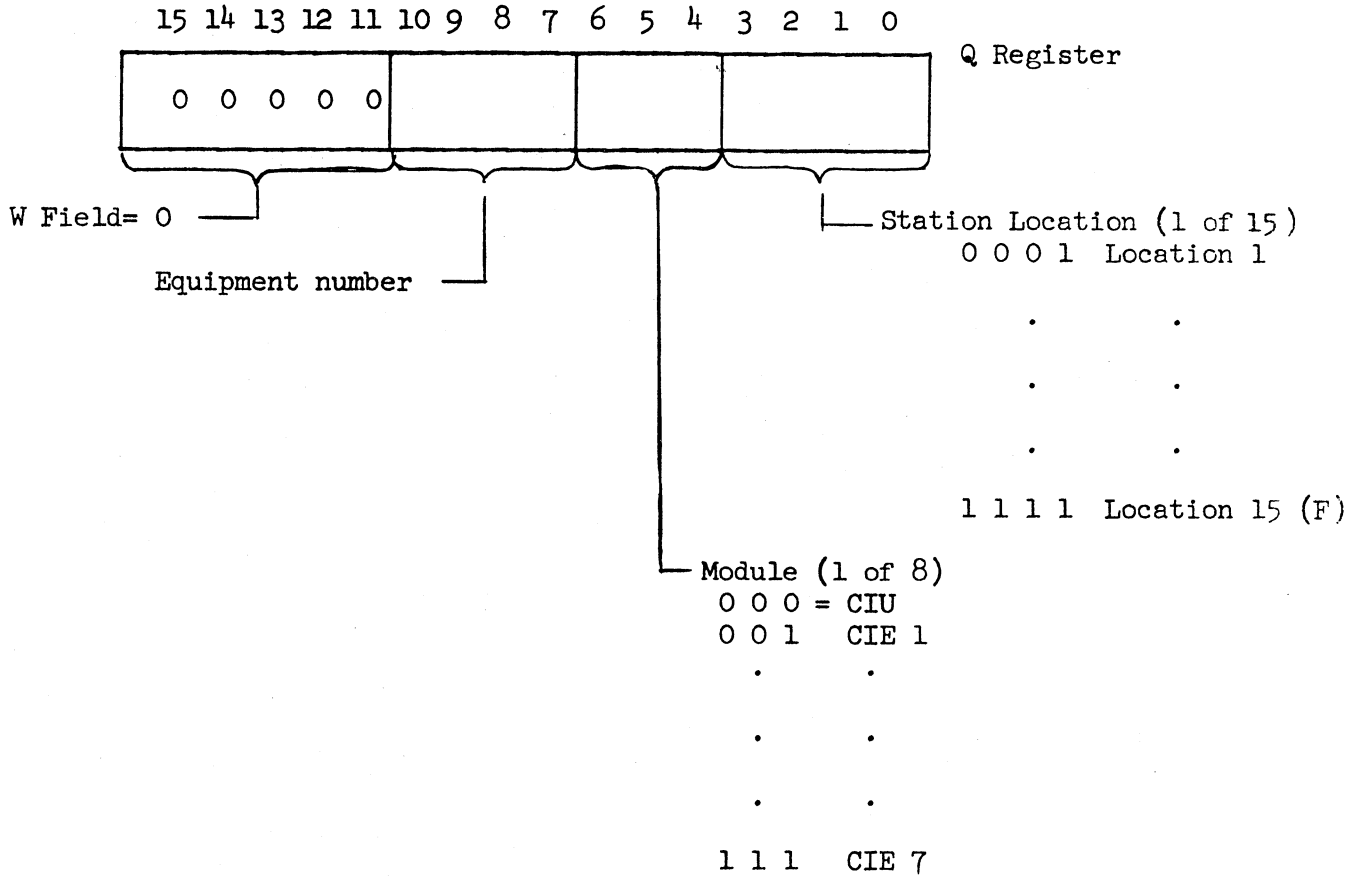
2.4 PROGRAMMING INFORMATION

2.4.1 GENERAL

The basic technique for generating I/O operations via the CIU/CIE is a direct connect mode with no continue feature. Station addresses are used to communicate with I/O unit devices. The CIU responds to two equipment code numbers: N and N+1, where N is even (i.e., 0 and 1, 8 and 9, etc.). Data transfers are performed on equipment number N and function/status operations on equipment number N+1.

2.4.2

Q--REGISTER DESCRIPTION



- Bits 0 - 3: The station I/O address; decoded for 1 of 16 station address locations in the module
- Bits 4 - 6 The module address; decoded for the CIU module or up to seven CIE modules in the system
- Bit 7: Function/Status bit contained in the equipment number
  - If 0, write operation loads station devices with data from the A register; read operation gates data from station device into the A register.
  - If 1, write operation loads station device with function command contained in the A register; read operation gates status from station device into the A register.
- Bits 8 - 10: The remaining bits of the CIU/CIE equipment number. The CIU responds to two equipment numbers: N and N+1, where N is even. Data transfers are performed on equipment number N and function/status operations on equipment number N+1.
- Bits 11 - 15 All zeros for the W field.

2.4.3

A-REGISTER DESCRIPTION

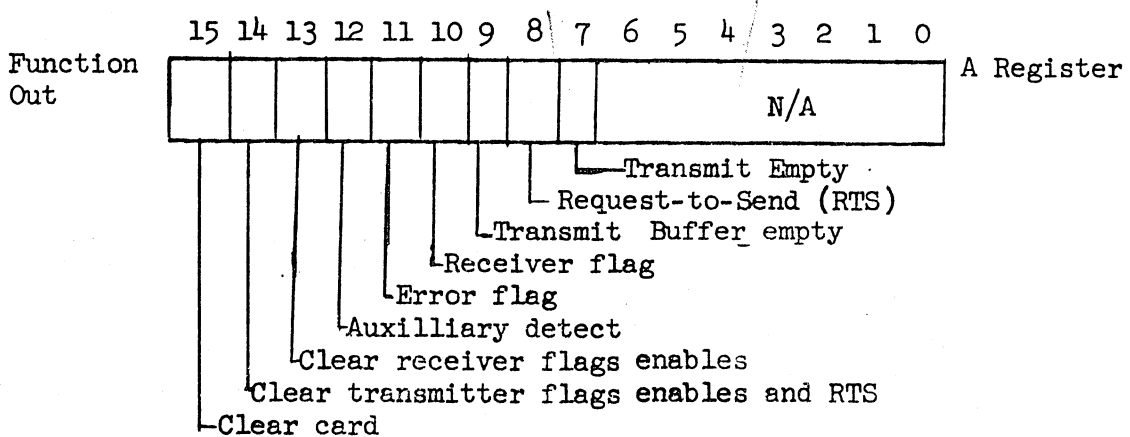
The A register is used to transfer all information to/from the SIO unit devices. The type of information contained in the A register is dependent upon bit 7 of the Q register:

- If 0 (data), bits 0-15 of A contain data to be transferred to/from the SIO station device during write/read operations
- If 1 (function/status), bits 0-15 of A contain, for write operations, function bits for setting up the SIO unit, and, for read operations, status from the SIO unit.

2.4.3.1

Function Write Operation

Bits 7-15 of the A register provide the write function operation to the SIO. The A register functions are as follows:



Bit 7: If set, enables the flag for interrupt to the CPU when the transmit section serial shift register is empty.

Bit 8: If set, enables the request to send signal for data write transfers to a terminal device or modem.

Bit 9: If set, enables the flag for interrupt to the CIU when the transmit section is ready to accept a data word.

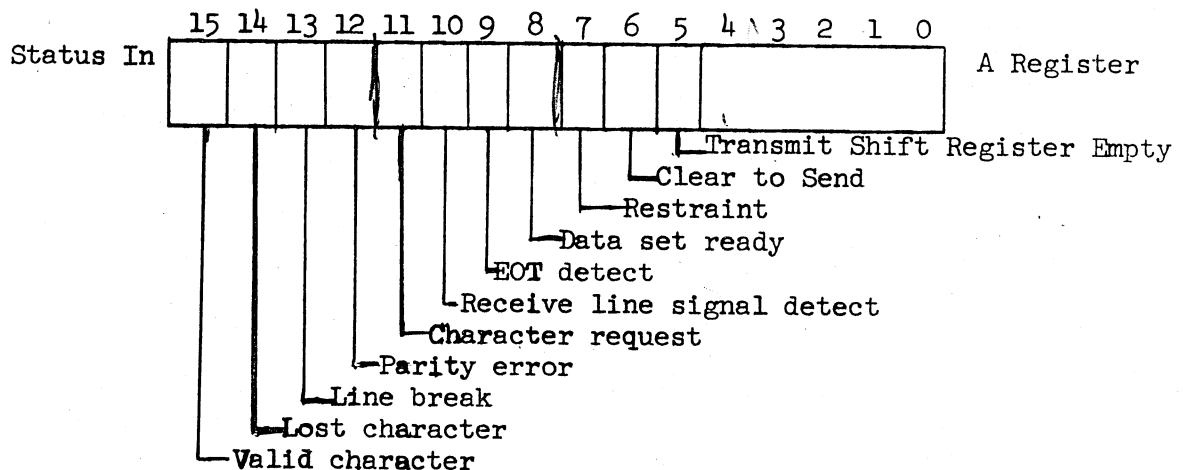
Bit 10: If set, enables the flag for interrupt to the CIU when a data character is received from an external device.

- Bit 11: If set, enables the flag for interrupt to the CIU on the following received data errors:
- Parity error (Incorrect parity)
  - Line break (absence of stop bit in character received)
  - Lost character (Two or more characters received without intervening read operation)
- Bit 12: If set, enables the flag for interrupt to the CIU when a preselected 5 to 8 bit character code has been detected.
- Bit 13: If set, disables receiver error, receiver, and auxilliary flags, and clears receiver flag enable flip flop.
- Bit 14: If set, clear the transmit flag and request to send flip flops.
- Bit 15: If set, provides a combined function of bits 13 and 14 and resets the entire card.

NOTE: All bits must be set to the desired state for each function command:  
 1 = enable function and 0 = disable function.

#### 2.4.3.2 Status Read Operation

Bits 5 - 15 of the A-register will contain the SIO card status on a read status operation. A description of the A-register status read is as follows.



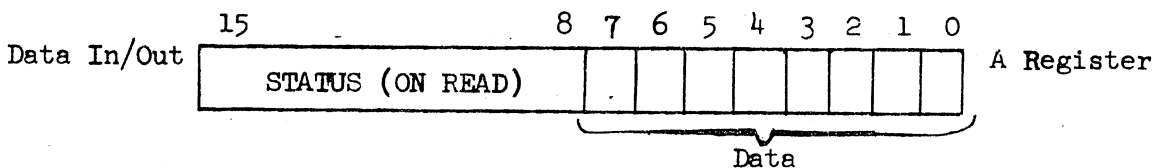
Bit 5: If set, indicates the transmitter serial shift register is empty.

Bit 6: If set, indicates the clear to send signal is valid.

- Bit 7: If set, indicates the external current mode restraint line is enable which will inhibit transfer of data from the CPU to the transmit section. Up to two characters can still be transmitted to the external device after restraint is enabled.
- Bit 8: If set, indicates ready status of external device or modem.
- Bit 9: If set, indicates that a preselected character has been detected.
- Bit 10: If set, indicates that a signal has been received from a terminal device or modem verifying it is receiving suitable data.
- Bit 11: If set, indicates that the transmitter will accept the next data word to be transmitted.
- Bit 12: If set, indicates a parity error condition occurred during a read data operation.
- Bit 13: If set, indicates absence of stop bit in received character.
- Bit 14: If set, indicates two or more characters received without an intervening read operation.
- Bit 15: If set, indicates that a complete character has been received.

2.4.3.3 DATA READ/WRITE OPERATION

Bits 0 - 7 of the A-register contain the received data (read) or data to be transmitted (write). Bits 8 - 15 will contain partial status information on a read data operation as defined above.



2.4.3.4 Interrupt Flag

The following conditions, if functionally enabled, generate an interrupt flag:

- Received character (Data available for read operation)
- Transmit Buffer Empty (unit is ready for next character)
- Character transmitted (Transmitter is empty)

- Error detect on received character
- EOT

The Interrupt/Flag is cleared by any one of the following conditions:

- Function disable
- Inverse buffer conditions of the transmitter or receiver that caused a flag
- Clear receiver flags and enables or clear transmitter enables
- Card master clear - All conditions

The interrupt flag line number is selected by nut/bolt jumper selection on the interrupt/flag status card of the CIU/CIE.

#### 2.4.3.5 Rejects

An external reject will occur on a write data operation if the transmitting buffer register (UART chip) is full.

An external reject will occur on a read data operation if the input buffer register (UART chip) is empty.

An internal reject will occur on an improper station address of the CIU/CIE.

#### 2.5. RESPONSE TIME

The response time of the SIO is dependent upon the serial I/O data communication rate (baud rate). Table 2.6 shows the typical response times for either a data transmit or receive character.

Table 2.6 Response Times

BAUD RATE	RESPONSE TIME/CHARACTER
19200	$\frac{1}{2}$ millisecond
9600	1 millisecond
4800	2 milliseconds
2400	4 milliseconds
1200	8 milliseconds
600	16 milliseconds
300	32 milliseconds
150	64 milliseconds
75	128 milliseconds

## 2.6 SAMPLE PROGRAM

The following is a sample machine language program (1700 Series Computers) which illustrates a closed loop test when serially transmitted data (card pin B19) is connected to serially received data (card pin B20) of the SIO with the RS-232-C jumper module inserted. Jumper RTS (pin B21) to CTS (pin B22) also.

```

E000 } Load Q with equipment number/function/slot location (slot 10
068A } arbitrarily selected).
C000 }
8000 } Load A with SIO CLEAR command.
OB00 }
03FE } Output A.
C000 }
0100 } Load A with SIO TRANSMIT ENABLE command. (RTS set)
OB00 }
03FE } Output A.
E000 }
060A } Load Q with equipment number/data. (Command slot location)
C000 }
0055 } Load A with data pattern
OB00 }
03FE } Output A.
C000 }
7FFF } Load A with initial count value.
09FE } Increase A.
0101 } Skip if A = 0.
18FD } Jump back to count.
18FA } Jump back to data output.

```

} 32 msec delay (accommodates 300 - 9600 baud rates).

## 2.7 TRANSMIT/RECEIVE CODE SET

Table 2.7 shows the transmit/receive code set of the 752-10 terminal. This is a standard ASCII 128-code set, consisting of 33 control codes (columns 0 and 1 and row 15 of column 7) and 95 alphanumeric character codes. The heavily outlined portion of the figure represents the 64-character ASCII subset of alphanumerics available when the 96/64 switch on the terminal keyboard is in position 64. Notice also that the table uses the traditional communications method of identifying bits b1 through b7, rather than the data processing method of b0 through b6.

BITS					COLUMNS									
b7	b6	b5	b4	b3	b2	b1	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	1	1	0	1	0	1	1
0	1	0	0	0	0	0	0	1	1	0	1	0	1	1
0	1	0	1	0	0	0	0	1	1	0	1	0	1	1
0	1	1	0	0	0	0	0	1	1	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	0	1	0	1	1
1	0	0	0	0	0	0	0	1	1	0	1	0	1	1
1	0	0	1	0	0	0	0	1	1	0	1	0	1	1
1	0	1	0	0	0	0	0	1	1	0	1	0	1	1
1	0	1	1	0	0	0	0	1	1	0	1	0	1	1
1	1	0	0	0	0	0	0	1	1	0	1	0	1	1
1	1	0	1	0	0	0	0	1	1	0	1	0	1	1
1	1	1	0	0	0	0	0	1	1	0	1	0	1	1
1	1	1	1	0	0	0	0	1	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1	1	0	1	0	1	1
0	0	0	0	0	0	0	NUL	DLE	SP	0	@	P	'	p
0	0	0	1	0	0	0	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	0	0	0	STX	DC2	"	2	B	R	b	r
0	0	1	1	0	0	0	ETX	DC3	#	3	C	S	c	s
0	1	0	0	0	0	0	EOT	DC4	\$	4	D	T	d	t
0	1	0	1	0	0	0	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	0	0	0	ACK	SYN	&	6	F	V	f	v
0	1	1	1	0	0	0	BEL	ETB	'	7	G	W	g	w
1	0	0	0	0	0	0	BS	CAN	(	8	H	X	h	x
1	0	0	1	0	0	0	HT	EM	)	9	I	Y	i	y
1	0	1	0	0	0	0	LF	SUB	*	:	J	Z	j	z
1	0	1	1	0	0	0	VT	ESC	+	;	K	[	k	{
1	1	0	0	0	0	0	FF	FS	,	<	L	\	l	:
1	1	0	1	0	0	0	CR	GS	-	=	M	]	m	}
1	1	1	0	0	0	0	SO	RS	.	>	N	^	n	~
1	1	1	1	0	0	0	SI	US	/	?	O	_	o	DEL

Table 2.7 752-10 Terminal Code Set

All codes shown in Table 2.7 may be generated and transmitted by the terminal. All codes may also be received by the terminal; however, a terminal only actively responds to the following 13 control codes:

<u>ASCII Mnemonic</u>	<u>Octal Code</u>	<u>Function</u>
BEL	007	Sound audible alarm for 250 ms
BS	010	Backspace cursor without affecting displayed data
LF	012	Move cursor down a line from present position without affecting displayed data
CR	015	Move cursor to beginning of current line or next line, depending on setting of internal AUTO LINE FEED switch
NAK	025	Move cursor ahead a character position without affecting displayed data
SYN	026	Clear line containing cursor from position of cursor to end of line; cursor does not move
CAN	030	Clear display memory and reset cursor to home position
EM	031	Reset cursor to home position without affecting displayed data
SUB	032	Move cursor up a line from present position without affecting displayed data
ESC	033	Idle character or X-Y positioning characters follow, depending upon position of internal X-Y positioning switch
SO	016	Advance cursor one position and initiate a low intensity field*
SI	017	Terminate a highlight field (low intensity or blink) and advance cursor one position*
ETB	027	Initiate blink field*

Control characters, other than those listed, act only as idle characters if sent to the terminal unless the INTERNAL TEST switch is in the enable position. In this case, a symbol is displayed for each control code received (see appendix for list of symbols); control codes, including those previously listed, do not perform any function other than displaying their associated symbol.

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\* These functions only occur in terminals having the highlight features installed.

## Section Three

### INSTALLATION AND CHECKOUT

#### 3.1 INSTALLATION REQUIREMENTS

The non-synchronous serial I/O card (SIO) is a one-card device, 7-3/4 by 9 inches in size. It can be inserted into any even-numbered slot location (slot 10 and above) of the Computer Interface Unit (CIU) or a Computer Interface Expander (CIE). Signals are connected between the SIO and the external device by connecting a cable onto the backplane of the CIU or CIE module at the odd-numbered slot location (SIO card location plus one). A power cable, supplied with each SIO card, is connected onto the backplane at the SIO card slot location (see Figure 3.1).

#### 3.2 POWER REQUIREMENTS

Logic power of +5 vdc is supplied by the CIU or CIE module. A +15 vdc power supply is also required and is provided by a standard power supplement to the CIU or CIE rack system.

The typical current required for one SIO card is as follows:

+5v	600	milliamps
+15v	75	milliamps
-15v	45	milliamps

Note: Primary power for the supplies is 115vac, 60Hz or 230vac, 50Hz.

#### 3.3 CABLING AND CONNECTORS

##### 3.3.1 POWER

A cable assembly, CDC No. 39970700, connecting ground and +15v is required to the even-numbered slot location where the SIO card is used. See Figure 3.1.

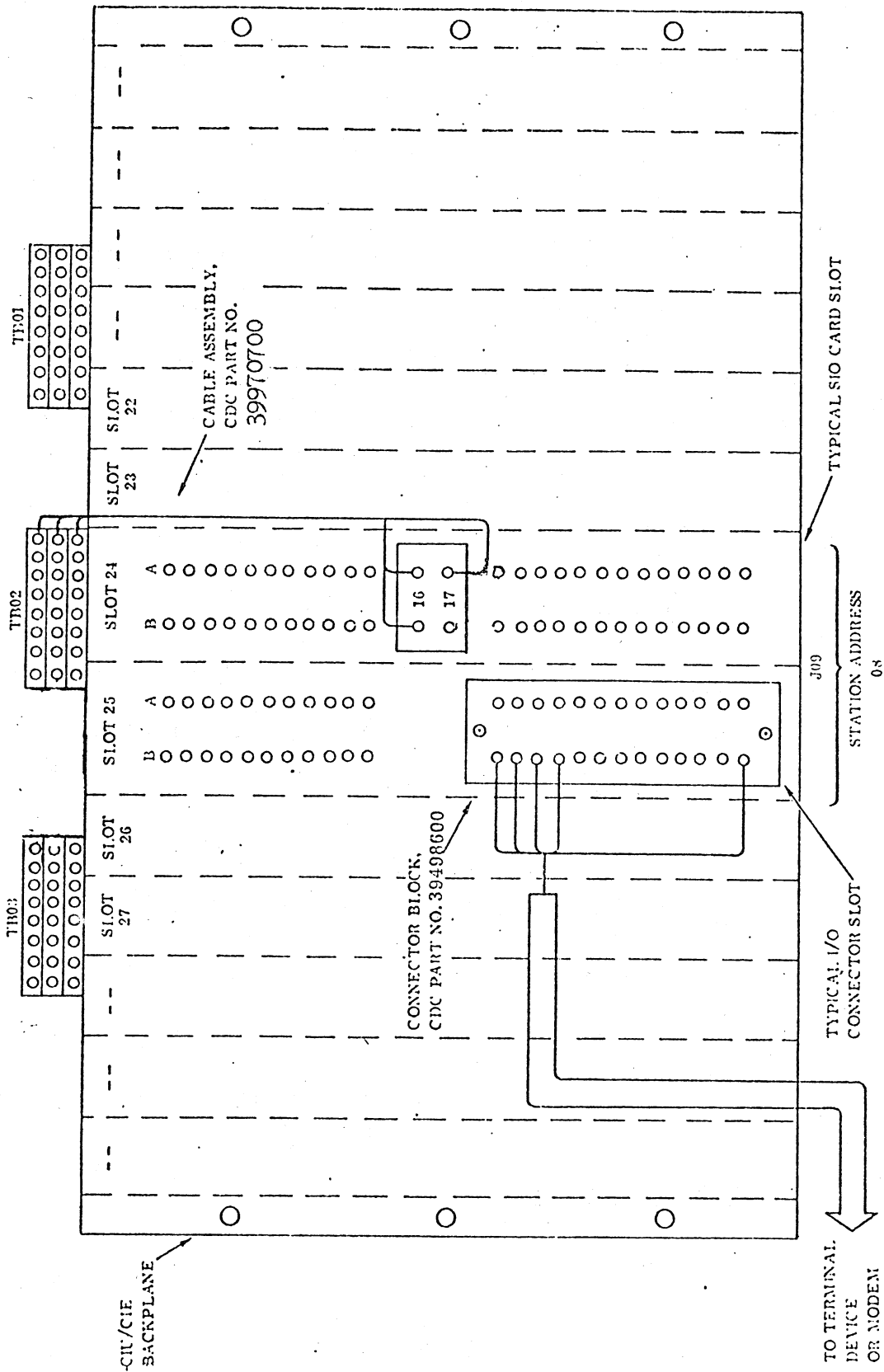


Figure 3.1. Backplane View of Signal and Power Cable Connections

### 3.3.2

#### EXTERNAL SIGNALS

External I/O signals are connected to the respective SIO card by placing a cable assembly on the rear of the CIU or CIE module at the odd-numbered slot location. A cable assembly, CDC Part No. 399174xx, is used when connecting to a modem. A cable connector kit, CDC Part No. 39932400, is required for interfacing with terminal devices other than modems. Items in the kit are:

- Connector Housing---CDC Part No. 39498600
- Connector Block-----CDC Part No. 94261810
- Contacts-----CDC Part No. 94245600

A Berg Electronics Inc., crimp tool number HT-66 is required for connecting the contacts to the customer-furnished cable. Figure 3.2 illustrates a recommended assembly for the input cable. Figure 3.3 illustrates a typical SIO card to terminal device interface cable.

### 3.4

#### INTERFACE CHARACTERISTICS

#### 3.4.1

##### CIU/CIE DATA/CONTROL BUS INTERFACE

The data/control bus between the SIO and the CIU/CIE module is described in the Computer Interface Unit/Computer Interface Expander Manual.

#### 3.4.2

##### EXTERNAL I/O INTERFACE

The signal and pin assignments for interfacing an external device are listed in Table 3.1.

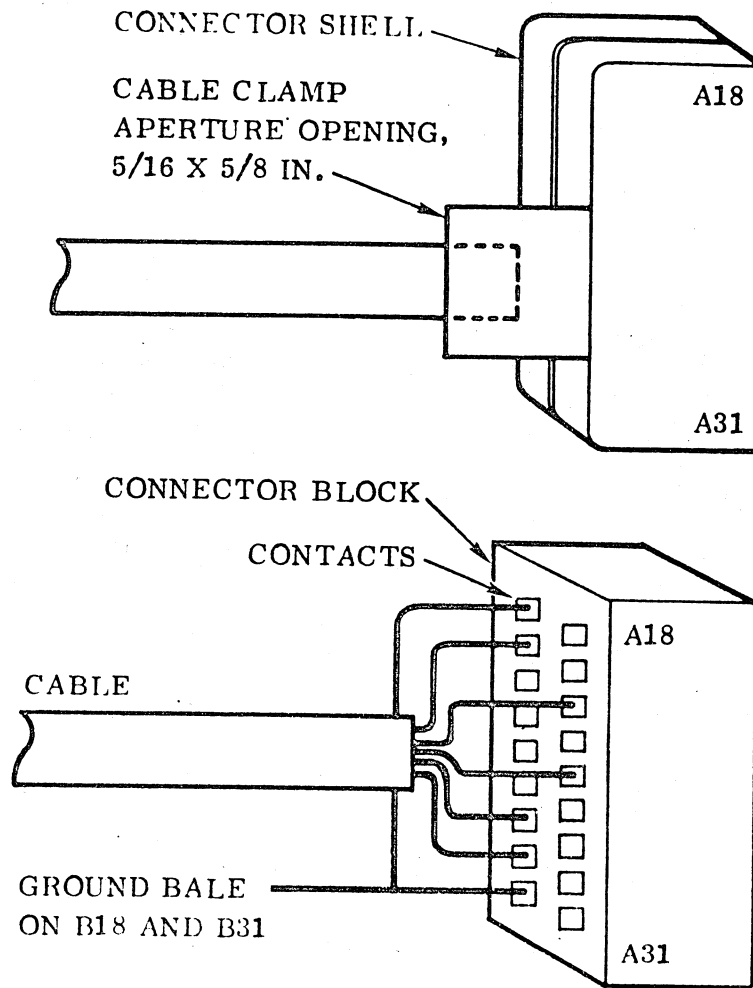
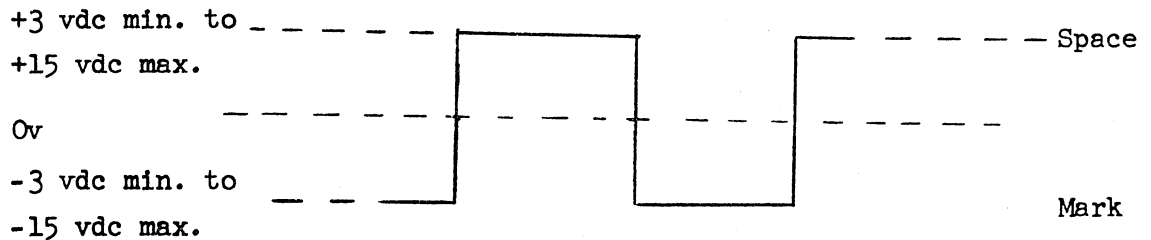


Figure 3.2. Input Cable Connector Assembly



### 3.4.2.1 Data Signal Levels

The RS232-C data communication signal levels for the data lines (TRDAT and RCDAT) are as follows:



The internal logic has a mark as a one and a space a logic zero.

The timing and control circuits (Request to Send, Clear to Send, Data Set Ready, Data Terminal Ready and Received Line Signal Detector) are defined as being ON when a space is on the line. Conversely, a -3 to -15 volt level on a control circuit line means the function is OFF.

Nominal interface signal levels for unipolar current/photo-diode operation are as follows:

Internal logic level	Loop Current
ONE (Mark)	20ma + 2ma
ZERO (Space)	0 to 0.1ma

Note: If the marking sense control jumper is installed (pin 13 to 16 of the jumper module), the current/photo-diode logic is reversed-i.e., a mark becomes no current flow and a space is 20ma. For bipolar operation current always flows but changes direction between mark and space.

### 3.5 Cooling Requirements

An air flow of 350 fpm is required across the SIO card in system applications to assure adequate component life. Standard air flow is provided when the SIO card is inserted in a CIU/CIE system.

3.6

ENVIRONMENTAL LIMITATIONS

See paragraph 3.6 of CIU/CIE manual.

3.7

PREPARATION FOR USE

Verify the (+15v) power cable is connected between TBO2 and A16, B16 and A17 on the backplane at the even slot position. Verify the UART switches (word length, stop bit, parity), the baud rate switches and the EOT (if used) switches are in their proper settings. Make certain the appropriate jumper module (see Appendix A) is seated firmly in its socket. Verify the appropriate cable is connected from pins 18-31 of the odd slot of the backplane to the external device.

TABLE 3.1. SIO EXTERNAL INTERFACE SIGNALS

PIN NUMBER	SIGNAL	RS232 SIGNAL	DESCRIPTION
A18	PDDL		Current receive data low*
B18	GRD	AB	Signal common
B19	TRDAT	BA	RS232 data transmit (current transmit data common)
B20	RCDAT	BB	Receive data RS232 (current receive data high*)
B21	RTSTR	CA	Request-to-Send transmit
B22	CLRTS	CB	Clear to send
B23	DSRDY	CC	Data set ready
B24	DTRDY	CD	Data terminal ready
B25	RLSD	CF	Receive line signal detect
A29	TRDAH		Current Transmit Data High Bipolar*
B29	TRDAL		Current Transmit Data Low Bipolar*
A30	RESH		Restraint receive high*
B30	RESL		Restraint receive low*
B31	GRD		Signal common

\* Current loop operation

## Section Four

### THEORY OF OPERATION

4.1

#### GENERAL

The non-synchronous serial I/O unit, connected in a Computer Interface Unit or Computer Interface Expander, provides a communication link between the control computer and a serial-data device. The serial I/O unit (SIO) consists basically of two sections, send and receive. Each section is controlled by either function writes, read/write data, or status read operations from the control computer via the CIU/CIE. Minature switches on the SIO card provide a wide range of general-purpose serial data communication applications. These include baud rates, character word lengths, parity and special character detection. Current loop/photodiode or RS232-C data communication capabilities are provided as alternate features on a component-swapping basis.

Table 4.1 contains a glossary of the terms used in this section.

4.2

#### PRINCIPLE OF OPERATION

A functional block diagram of the SIO unit is shown in Figure 5.1.

Information flow in this block diagram has basically four paths which are:

- ① Parallel data from the computer via the CIU/CIE
- ② Serial data and control to a terminal device or modem
- ③ Serial data and control from a terminal device or modem
- ④ Parallel data to the computer via the CIU/CIE

The nucleus of the SIO operation is the MOS/LSI Universal Asynchronous Receiver Transmitter (UART) which performs the parallel-to-serial conversion for the send logic and converts incoming serial data to parallel for transmission to the CPU on receive operations. Operating conditions are established by DBO7-DB15 during a function write.

A data write will load DBO0-07 into the buffer register of the UART which, in turn, will add the appropriate parity and stop bits and transmit the data serially. The serial data may be either RS232 voltage levels or current loop depending on the system application.

Serial received data may also be either RS232 voltage level or current loop, depending on system application. The UART checks the parity and stop bits and converts the serial input to parallel data for input to the CPU on a read data operation.

The status of the SIO card and the communication facility is sent to the computer on a status read operation. The serial bit times are selected (separately for send and receive) by the baud rate generator logic.

## 4.3 DETAILED THEORY OF OPERATION

### 4.3.1 UART

In general, the operation of the UART is controlled by the inputs to its control register (word length, parity and stop bit select) which are strobed by the load mode register signal. Provided the UART is in a reset state (no data to be transmitted), the control register can be set allowing selection of the number and type of data bits, parity and stop bits for both the send and receive sections. For SIO operation, the control register strobe is wired high and the control register inputs are controlled by switch S3. Thus, as soon as the power master clear pulse is generated, the SIO is set to the desired mode of operation. The UART has two transmit status outputs (input buffer empty and transmitter empty)

and four receive status outputs (receive data available and parity, overrun and frame errors) that are controlled by the status strobe at pin 16. For the SIO, the strobe has been hardwired (in this case to a low) to allow status to always be available.

The operation of the UART during transmit operations is the following. After reset, the transmit clock at 16x baud rate is applied and data are loaded into the transmit buffer register with a data write which becomes the negative-going load buffer register pulse at pin 23. The UART will send serially a start bit, the selected number of data bits, a parity bit (if selected) and the required number of stop bit (s). Note that if less than 8 data bits are selected the unused bits are ignored. The data is right justified such that DB00-04 are always transmitted. A further point is that if the UART is programmed for 2 stop bits and the word length selected is 5 bits, the UART will actually output a 1.5 stop bit. This closely approximates the 1.42 stop bit for the 5 bit Baudot code.

Assuming the receive clock at 16x the baud rate is input, the UART will begin searching for a start bit on receive as soon as the reset signal has gone. Reset leaves the error flags and the receive register full status lines at a low level. After receipt of a valid start bit, the UART shifts in the number of bits selected by the word length control, tests for parity (if selected) and checks for the programmed number of the stop bit (s). The UART will test for and set error flags if parity, framing or overrun errors are detected. Depending on the control register, the receiver will test for even, odd or no parity. A framing error flag will be set if, after detection of a start bit, no stop bits are found. This condition also can indicate a line break. An overrun error flag is set if two consecutive characters have been received and the first character has not been read into the computer. The fourth receive flag is receive register full which is

set when a full character including stop bit (s) has been received and transferred to the receive buffer register. When the receive data is read from the UART, a low level signal is applied to pin 18 which resets the receive register full signal and prevents generation of an overrun error. The computer has a full character time to read the receive data after first character was received before an overrun error can occur. If less than an 8 bit word length is programmed, the data will be right-justified and the unused bits will be at low levels (logic zeros). Thus, receive register bit 1 is the least significant bit and bits 1 to 5 will always be present. However, bits 6 through 8 may be logic zeros depending upon the word length programmed.

For further information on the UART, see Section VII-Parts Data

#### 4.3.2

##### Dual Baud-Rate Generator

Generation of the 16x baud rate clocks is accomplished by a crystal-controlled oscillator. Each half of the baud-rate generator is basically a programmable 15-stage feedback shift register which is capable of dividing a modulo up to  $(2^{15}-1)$  or 32k. The chip contains a Read-Only Memory (ROM) that is pre-programmed to provide the shift register with appropriate counts to generate a pulse trains at 16x times a set of asynchronous baud rates. The ROM is programmed to allow division of the crystal frequency by 32, 64, 128 . . . etc to give 16x the baud rate of 19200, 9600 down to 75 baud. In addition, frequencies of 16x baud rates of 50, 110, 134.5, 1800, 2000, 3600 and 7200 baud have been programmed. Selection of appropriate one of 16 possible frequencies is accomplished by a 4 bit address for each half of the baud rate generator. The two halves of minature DIP switch S2 are used to select the transmit and receive clocks for the UART at 16x the baud rate. **Section 2, Table 2.4, lists the switch position vs baud rates.**

### 4.3.3 Function Write

As described in Section II, if the equipment field is odd (Q7=1), the computer is requesting a function or status. When the station (slot) address is correct with Q7=1 and the computer generates a write, the inputs to the lower gate of A7 are all enabled causing the function strobe (N) to go high. The function strobe gates DB07-12 to their respective flip flops setting the flag enables. DB08 sets the Request to Send flip flop which gates this signal through an RS232 level converter to an external terminal or modem. This enables the external device so when it returns Clear to Send (RS232 operation) the transmit section can request data allowing transmission to begin. DB07 and 09 set the flag flip-flops to enable the UART to generate a Tx flag (II) when the UART serial shift register or the buffer register, respectively, are empty. The buffer register empty flag/interrupt is used to request a new character for transmission while the shift register flag/interrupt lets the program know all the data has been transmitted. DB10, 11 and 12 set the Rx enable flip flops for buffer full, error or special character flag/interrupts. The buffer full flag/interrupt signifies a full character has been received and needs to be read before an overrun error occurs. The error flag/interrupt will occur if a parity, frame or overrun error is detected. The special character (EOT) flag/interrupt will occur when a received character matches that set in switch S1. DB 13 and 14 and function write clear the Receive and Transmit functions respectively, that were previously set. Function write with DB 15 set clears the entire SIO card including the UART.

#### 4.3.4 Function Read (Status)

When  $Q7=1$  and a read input operation is programmed by the computer, the SIO will present its status on DB05-15. READF at the left of logic sheet 2 is inverted and ANDed with Function  $\textcircled{Q}$  and station  $\textcircled{S}$  to generate a status enable signal. The status enable ORed with Read data gates status onto the DB 08-15 lines. A separate status enable  $\textcircled{SE}$  gates status to DB05-07 on function read only. The three error flags and the buffer full signal are gated from the receive section of the UART to DB 12-15. The buffer empty and shift register empty flags of the transmit section of the UART are gated to DB11 and 05 respectively. DB06, 08 and 10 (the Clear to Send, Data Set Ready and Receive Line Signal Detected, respectively) are the RS232 interface controls returned from an external terminal or modem. DB07 is the status of the external restraint signal which can be used in current loop operation. DB09 is the special character (EOT) detected flag. The status lines are 202 elements which are open collector circuits which have collector resistors supplied by the CIU/CIE bus receivers.

#### 4.3.5 Data Write

When  $Q7=0$  and a write (output) operation is programmed by the computer data can be written to the SIO provided the transmit buffer of the UART is empty. If the Tx Buf Empty  $\textcircled{G}$  or  $\textcircled{FF}$  is high and there's no restraint (CLR to Send and Restraint are high), the data input to the Tx Ready flip-flop (sheet 1) is enabled. The computer will load a character by doing a data write which will enable the upper gate of A7 and generate a positive-going pulse to clock the data into the Tx Ready flip-flop. The  $\overline{Q}$  side  $\textcircled{VV}$  is sent to a one-shot (sheet 2) which generates a one  $\mu$ s signal  $\textcircled{AT}$  which is sent to the two-input NAND C6. The output of this gate is a one  $\mu$ s negative-going pulse which is used to clock the character on DB 00-07 into the UART. If the computer should try to load a character

and the Transmit Buffer Register is not empty, two things would occur. One, a reject would be generated from the logic on Sheet 2 and also, the Inhibit Tx Request signal would be high keeping the Tx Ready flip-flop reset which would allow no strobe to the UART. If less than eight bits have been selected as the data word length, the unused bits (DB08, 07 etc) will be ignored by the UART. The Transmit ready flip flop which controls the data write operation has the slot (station) address signal (S) as its reset signal. Thus, as soon as the computer finishes addressing the SIO card-i.e, after completing a read or write - the Tx Ready signal will be reset. The two 202 open collector gates shown in the upper right area of Sheet 1 are wire-ORed to generate the Transmit Flag (II) signal. If enabled by function with DB09 true, the output A3-6 will go low when the Tx buffer is empty and there's no restraint. If enabled by a function with DB07 true, A3-8 will go low when the Tx Shift Register is empty.

#### 4.3.6

##### Data Read

When Q7=0 and a read (input data) operation is programmed, the received serial data can be input to the computer provided there is data in the UART's Receiver Register. Logic diagram sheet 2 contains most of the logic for data read operations. When a full character is received by the UART, the Receive Register Full (AF) signal is set high. If the Rx Flag flip flop has been set by a function with DB10 set, the Rx Buffer Full signal will cause the Rx Buffer Flag (BB) from A4-6 to go low and generate a flag/interrupt signal. After reading the status to determine that receive data is ready, the program will do a read (input data) instruction. Read, in conjunction with Function (data) and the correct slot (station) address, will enable the 4 input NAND, C7, causing C7-6 to go low. C7-6 is inverted by two separate inverters and their outputs, C2-4 and C8-10, then become Read Data.

C8-10 gates the received data onto the bi-directional DB00-07 lines while C2-4, in conjunction with the Rx Buffer Full (FB) signal, sets the Rx Ready flip flop. When read is complete, Rx Ready (AR) goes high which triggers a 300ns pulse (RR) which goes to the UART to avoid an overrun error. (AR) also enables the reply logic shown in the lower left corner of sheet 2. This logic causes the reply to be delayed by one  $\mu$ s to provide time to service the UART and allow the status inputs to settle. If the computer should try to read and the Rx Buffer is empty, the Rx Ready flip flop will not set causing B5-3 to go low and generate a reject. Note that a read data operation will also enable the Read and status line (TP19) to put status on bits 08-15 of the data bus. Thus, after a operation the computer will have data in the lower 8 bits and status in the upper 8. To read the status of the Restraint, Clear to Send or Tx shift Register Empty signal a function read rather than a data read must be programmed.

#### 4.3.7 Flag/Interrupts

The SIO has the capability to set a flag (or if set up in the CIU/CIE, generate an interrupt) for any of eight situations if properly enabled. All eight are ORed to a single flag/interrupt line at P1-A13. There are five flip flops (register bits) which enable the flags. The transmit portion of the UART has two signals- Buffer Empty and Shift Register Empty- which can generate a flag. The two Tx flags are wire ORed by the 202 gates of A3 to generate the Tx Flag (II) signal. The Rx Buffer Full signal, if enabled by the Rx Flag flip flop, will generate the Rx Buffer Flag (BB) signal. If the EOT Flag Enable is set and the special character is detected by the 524 elements on sheet 3, the EOT flag will be set. Enabling the Rx Error flip flop will allow any of the receive errors (parity, Line Break or Frame Error and Overrun or Lost Character) to generate a flag. E6-6 (TP24) is the output of a 4-input OR gate which will go high if any

of its flag inputs go low. The output is inverted at D5-10 and sent to the interrupt flag status card in position 7 of the CIU and CIE modules.

#### 4.3.8 Reply/Reject

The lower portion of sheet 2 contains the reply/reject logic for the CIO. The A6-12 output is the reject signal which will be high if the computer tries to load the Tx buffer and it is still full (Z) or a read data operation is attempted (B5-3) and there is no data in the receive buffer register. The reply logic is designed to provide a one  $\mu$ s delay for data read and both data and function write operations to allow the UART to be steady state. An instant reply is generated if a status read is programmed. If a data read or write is done with the UART in the proper state or a function write is programmed, one of the inputs to a three-input OR, A6, will go low causing A6-8 to go high. This will trigger the one  $\mu$ s one shot, B7, and will enable C6-1. While the one-shot is on, the false output will delay the reply gate output, F6-6, for one  $\mu$ s. Note the status reply is not delayed.

#### 4.3.9 Special Character (EOT) Detect

Switch S1 and the 524 gates on sheet 3 and the EOT flip flop on sheet 2 are the elements in the special character detection logic. Because this logic is most used to detect an end-of-text character, it is also named the EOT circuitry. S1 is set up with data bits 0-7 to select a particular character. When this character is received in the Receiver Buffer Register, the comparison is made by the 524 elements and the EOT Detect (AE) signal goes high. To compare the 4 bit input at the top (8-4-2-1) must exactly compare with the lower (8-4-2-1) bits. When the character is input by a read data operation, the EOT flip flop is set which generates a flag if enabled and sets status bit 09 true. Since there is a one  $\mu$ s delay on reply, when the computer reads the data the EOT status will be a steady one. There is a

potential problem with respect to the word length selected for the UART. If less than eight bits are selected as the word length, the unused bits 8, 7, 6 etc will be logic zero for all received characters. To make the comparison valid the corresponding switch position must be a zero. As may be seen from sheet 3, the switches generate a high (one) when off and a low (zero) when on so the corresponding switch positions to the unused bits must be on.

#### 4.3.10 RS232 Transmit

The SIO has the capability to transmit data and provide limited interface control signals as defined by the EIA RS232-C standard. The RS232 signals from the SIO come from the 900 element at D7 shown in the upper right portion of sheet 1. The 900 element is a 1488 type and its description is in Section VII. The operation is such that high and low inputs to the 900 result in outputs of -12V and +12 Volts, respectively. One point to remember is that RS232 defines the data signals and control signals differently. For data circuits a signal more negative than -3volts is defined as marking (logic one) while a signal more positive than +3 volts is a space (logic zero). The interval between -3 and +3volts is the transition region and is not uniquely defined. For timing and control functions, when the function is off the signal is less than -3volts and an "on" function will have signal level greater than +3volts. As an example, the data terminal ready signal will be at +12 (function on) so long as the SIO has power on. The Transmitter Serial Output data from the UART is double-buffered and sent to D7-2 with the same logic sense. Thus, the normal high output from the UART when not transmitting data will put a -12V level (mark ) on the line.

#### 4.3.11

#### RS232 Receive

Four RS232 Signals are received and converted to logic level signals by the 901 element (1489 circuit) shown on the upper left portion of sheet 3. If the SIO is set up for RS232 operation, the jumper module will have a jumper from E8-6 to 23 which allows receive data from P1-B20 to be input to pin 13 of F7. In addition to RCDAT, three control signals (Data Set Ready, Receive Line Signal Detected & Clear to Send) are also input to the F7 chip. Section VII has a description of the 1489 circuits but essentially it's a Schmitt Trigger with a variable threshold. Only the data circuit (pins 11 and 13) use the variable threshold. By biasing the circuit with a 5k resistor to +5volts, fail-safe operation of the data line is available. If the data line which is normally marking (Vin more negative than -3v) should open, the output, F7-11, which goes directly to the UART (V) will go to a low level. This in turn, will cause the UART to eventually generate a line break. The other lines have an open control which will cause the control signals to output a high (logic one) if these lines should open. However, since the controls are inverted by the E7 circuits, the final outputs will be zeros. In normal operation both variable and open threshold circuits will output a logic high for an RS232 mark (<-3v) input and a logic zero for an RS232 space (>+3v). Note that should the RS232 cable fall off the fail safe operation can cause two events to occur. One, the receiver will generate a line break and the Clear to Send signal will inhibit data transmission if the restraint logic is enabled.

#### 4.3.12

#### Current Loop Conventions (Marking Control)

Although current loop predates RS232 operation, there is no standard defined. However, there is a Teletype<sup>(R)</sup> convention that has been used for many years. In this convention, a logic one is marking which is defined as current flow in the loop. A zero is a space whereby no current flows in the loop. When

(R) Trademark of Teletype Corporation

a line is not transmitting, the line is marking or current is flowing. In this convention the start bit is a space and the stop bit (s) are mark (s). Note a line break generate a space. Since a quiescent line is marking or current flows, a space is used as a flag to signal a start bit, an open line or in some special cases a function (normally reverse channel or restraint) is on. Although many variations of voltage and currents exist, most data processing devices run on 20ma loops with voltages of 5 to 28 volts. Not all peripheral devices follow the Teletype convention; however, when they do deviate, they generally switch the logic assignments such that a logic one becomes no current flow and a zero is current flow. The rationale is that the circuits dissipate no power in the quiescent condition. The SIO handles this inverse convention by inverting the input and output within the logic by changing the marking control. This logic is shown in Figure 4.1

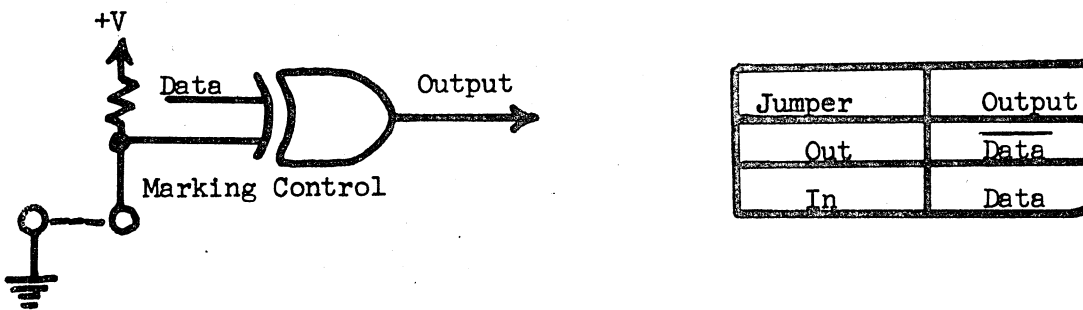
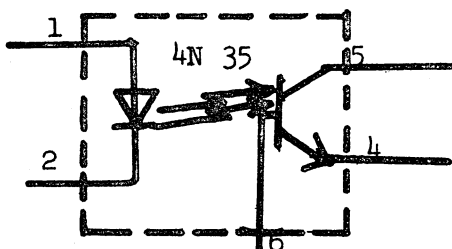


Figure 4.1 Marking Control Logic

When the jumper is out (normal convention), current flow in the loop is a logic one. When the jumper is in, current flow then defines a space (zero) and no current flow is a mark (one). The jumper, if needed, would go between pins 13 and 16 of the jumper module.

#### 4.3.13 Optoisolator Operation

The optoisolator circuit used in current mode operations looks as follows:



See Section VII for device specifications

When a signal is applied to the light-emitting diode (LED), it will generate a light with intensity proportional to the input current. The output photo-transistor detects the light and outputs a current that is also proportional to the light intensity. The ratio of the transistor output current to the diode input current is the DC current transfer ratio and runs from 40 to 100% for the 4N35. As the only connection between the input diode and the output transistor is the light from the LED, the input and output are electrically isolated from each other. In the SIO, two 4N35's are used to isolate the SIO current mode receive circuits from external transmitters while two other 4N35's are used to isolate the current mode transmitter from the logic.

#### 4.3.14 Current Loop Receive Circuits

The current loop receive circuit in simplified form looks like figure 4.2.

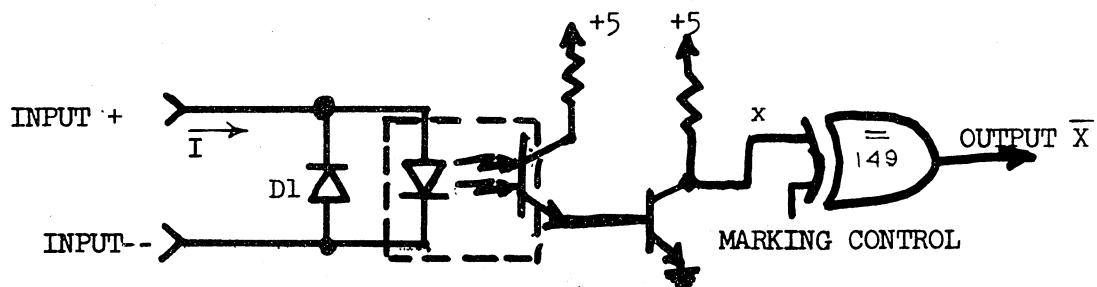


Figure 4.2 Current Loop Receive Logic

Current Flow,  $I$ , causes the LED to emit light allowing the phototransistor to turn on which presents a low level to the Exclusive Or (149) gate. With the marking control jumper ~~not~~ in, the output is inverted or is a logic one for this case. For no current flow, the LED is dark so the input to the 149 element is high and the output is low or a logic zero. If the marking control jumper is used the output is X or inverted from normal. D1 keeps reverse voltage to about 0.7 volts to avoid breakdown of the LED. In the actual receive circuit, there is also a resistor to limit loop current and provisions to power the loop.

#### 4.3.15 Unipolar Current Loop Transmit

A simplified diagram of the unipolar current loop transmit circuit is shown in Figure 4.3.

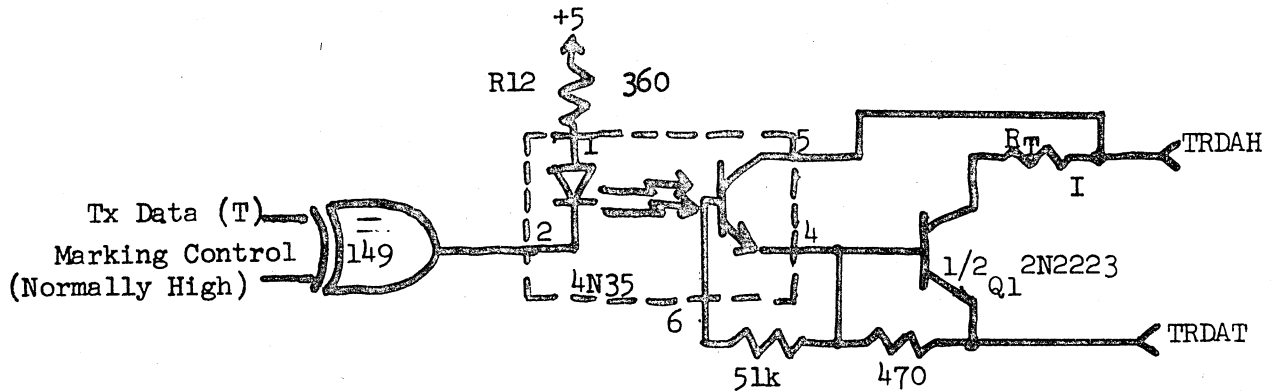


Figure 4.3 Unipolar Transmit Logic

Tx Data which has the same logic sense as the serial output data from the UART will be inverted by the Exclusive Or gate provided the marking control jumper is not used. When the UART output is high (marking), the output of the Exclusive Or will be a low level signal and the LED will be turned on. In turn, the output phototransistor and the drive transistor will be turned on and current will flow in the output loop. If the marking control jumper is in the output of the Exclusive Or gate is inverted so a logic one from the UART causes no current flow in the transmit loop. The main restriction on the transmit circuit is the speed at extended cable lengths. The 51k resistor from the base to emitter allows the circuit to operate at the higher baud rates. With a 12v, 20ma loop, the unipolar circuit will drive up to 1000 feet of twisted pair cable at 9600 baud. Note that  $R_T$  which is on the jumper module is selected to limit the loop current. Note that if the loop is powered by an external supply, the output loop is completely isolated from the internal SIO circuitry. As a corollary, if the SIO powers the loop, the +12v supply and its ground must be inserted in the loop and the isolation is reduced.

#### 4.3.16 Bipolar Loop Transmit

A simplified diagram of the bipolar current loop transmit is shown in Figure 4.4.

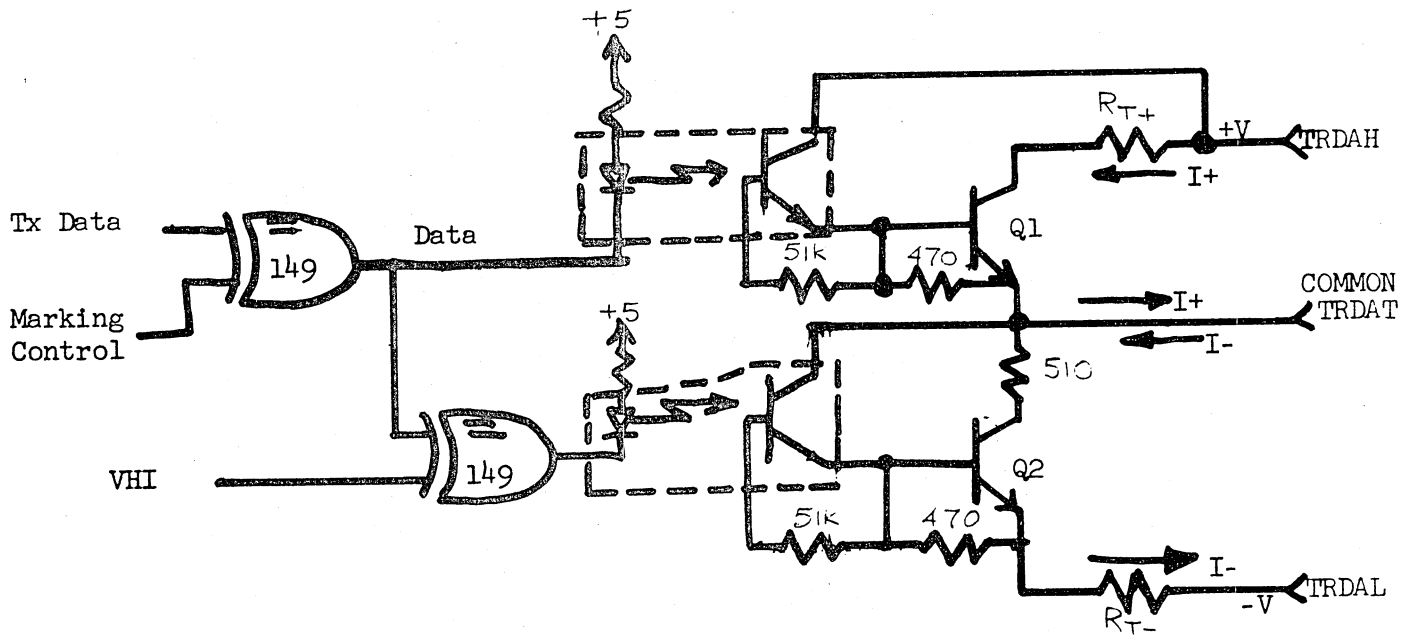
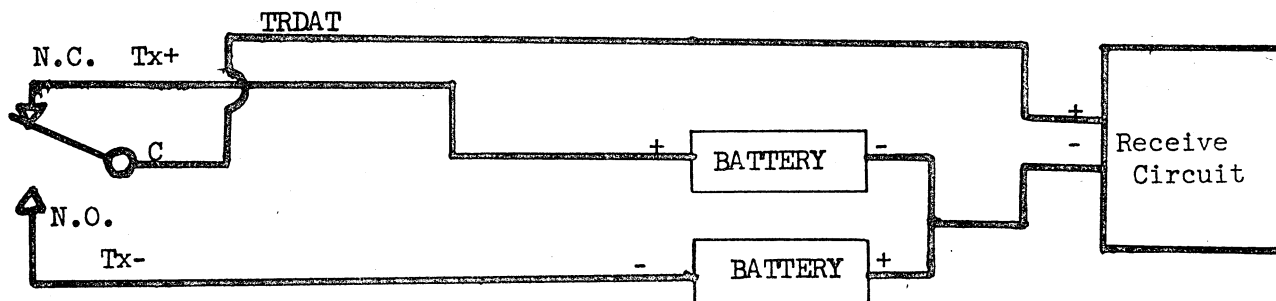


Figure 4.4 Bipolar Transmit Logic

The upper set of circuitry is that discussed in Section 4.3.13 above. Bipolar operation uses two loop supplies - one positive and the other negative - to drive very long lines with current loop operation. For one sense (mark arbitrarily), Q1 is switched on and current flows from the +V supply to the remote terminal as shown as I+. For a space, Q1 is shut off and Q2 turned on and current I- flows in the opposite direction. Because the current is pumped in two different directions, the signal may be rapidly switched even with long cables. The second Exclusive Or gate is set up to invert the data enabling the unipolar logic. Thus, one of the two LED's will be on at all times. This means the receive circuit will see either I+ or I- at all times unless there is a line break which causes no current flow. Note that bipolar transmission will work well with a unipolar receiver circuit (similar to the SIO's) provided the receiver has protection for the negative voltage, -V.

As shown in Figure 4.2, diode D1 will protect the LED against a negative voltage. The receive circuit would have the common output, TRDAT, and the common point of the power supplies as its two inputs. This is shown in a simplified form as follows.



The SIO can accept externally supplied voltages for maximum isolation or can use its internal +12v supplies in which case the receiver gets TRDAT and SIO ground as the two inputs.

#### 4.3.17 Restraint Logic

Three-input NAND gate, A6, in the lower right corner of sheet 1 is the transmit restraint control. Unless restrained by Clear to Send (RS232) or Restraint (Current Loop) when the Transmit Buffer Empty signal goes to a one, the Tx Ready flip flop is set enabling a new character to be transferred from the computer to the UART. For RS232 operations, the Clear to Send signal from an external device may be used to restrain the logic provided the jumper is in from pins 14 to 15 of the jumper module. For current loop operations, the Clear to Send jumper is left out but an external restraint circuit can be used.

The restraint logic is associated with inputs RESH, RESL and F8. In addition, soldered wire jumpers E9-E14 are associated with the current loop restraint logic. If a jumper is soldered from E13 to E14 the current loop restraint signal will be enabled. Further, if an external loop supply is used E9 to E12 would need to be jumpered. In this configuration, the current loop restraint circuit looks like the current loop receive as shown in Figure 4.2 of section 4.3.12. Provided the marking control is high (no jumper), current flowing in the restraint loop will generate a high signal on the Restraint (A) line. To restrain transmission, an external device will open the restraint loop (space) which will inhibit further character transfers from the computer to the UART Tx Buffer. As before if the marking jumper is in, the sense changes such that no current flow is normal and a current flow causes restraint.

NOTE: Enabling either Clear to Send or Restraint to inhibit transmission does not cause an instant stop. Instead, the transmitter will continue to transmit until it runs out of data. Up to two characters may be transmitted after the restraint is enabled so the external device must be capable of accepting two more characters after it has requested a restraint.

#### 4.3.18 Reset

The SIO has four signals which can clear portions of the card. A function write with DB 13 set will clear the three receiver flag enable flip flops. A function write with DB 14 set will clear the transmitter flag enables and the request to send signal. A function write with DB15 set or a Master Clear from the computer will clear the entire card including the UART.

NOTE: Resetting the UART clears the Status and Transmit portions but may not clear the receive buffer register depending upon the UART type.

## Jumper Module

The major mode (RS232 or current loop) of operation and auxiliary control selection is accomplished by a 28 pin jumper module that plugs into a mating socket at E8. Sheet 3 of the logic shows the connections to the socket. Although the drawing is somewhat crowded and difficult to follow, it can be seen that jumpers are designed to go directly across from the left side to the right side in most cases. The upper portion of the module (pin 1-12 and 17-28) are concerned with transmit and receive data. Pins 13 and 16 are involved if a marking sense change is required and pins 14 and 15 control the use of Clear to Send as a restraint on RS232 operations. The upper five positions (pins 1-5 and 24-28) are associated with the transmit data outputs. Jumpering pin 1 to 3 puts RS232 Tx data on the output lines. The remaining pins are associated with current loop operation and pins 3, 5 and 28 are the transmit outputs for this mode. The next five positions (pins 6-10 and 19-23) are associated with bringing the receive data from the input line to either the RS232 or current loop receive circuits so the data may be converted to logic levels. The data input, RCDAT, from P1-B20 is connected to pin 6 so that a jumper to either pin 23 (RS232) or 22 (current) will connect the appropriate receive circuits. The remaining pins are associated with current loop operation and, specifically, pin 19 is connected to P1-A18 which is the other lead for current receive data. Pins 11, 12, 17 and 18 take the logic level outputs for receive data and connect to the receive serial data input to the UART. To input RS232 data pin 11 is jumpered to 18 while current loop requires a jumper from 12 to 17. Current limiting resistors for current loop operations may also be found on the jumper module between pin pairs 2/27, 5/24 and 8/21. For a more detailed explanation of the jumper module see Appendix A.

Table 4.1 Glossary of terms

TERM	DEFINITION
Baud Rate	Data communication rate
Character	Serial data word consisting of a start bit, 5 to 8 data bits, an optional parity bit and one or two stop bits.
CTS, CLRTS, CLR to SEND	Clear to Send from external device
DBOOF - 15F	Data bits 00-15 false (to/from the CIU/CIE common bus)
DSRDY	Data set ready from external device
DTRDY	Data terminal ready from SIO
EOT Detect	Special character (end-of-text?) detected
FLXXF	Flag line false (to bus)
FUSTF	Function/status false (from bus)
MCLRF	Master clear false (from bus)
PDDL	Photo diode low (cathode) of receive current loop
RCDAT	Receive data (RS232) or photodiode high (anode) of receive current loop
READF	Read false (from bus)
RESETF	Master clear or card clear
RESH/RESL	High (anode) and low (cathode) inputs to the photodiode in the current loop restraint circuit
RESTRAINT	Current loop signal to inhibit data transmission
RJCTF	Reject false (to bus)
RLSD	Receive line signal detected from external device
RPLYF	Reply false (to bus)
RTS, RTSTR	Request to Send from SIO
SSXXF	Station select false (from bus)
TRDAH/TRDAL	Transmit data output High/Low from current loop transmitter
TRDAT	Transmit data (RS232) or data output common from current loop transmitter
UART	Universal asynchronous receiver transmitter
WRITEF	Write false (from bus)

## Section Five

### Diagrams

#### 5.1 General

This section contains the following diagrams:

<u>Figure No.</u>	<u>Title</u>
5.1	Serial I/O Block Diagram
5.2	Serial I/O Logic Diagram

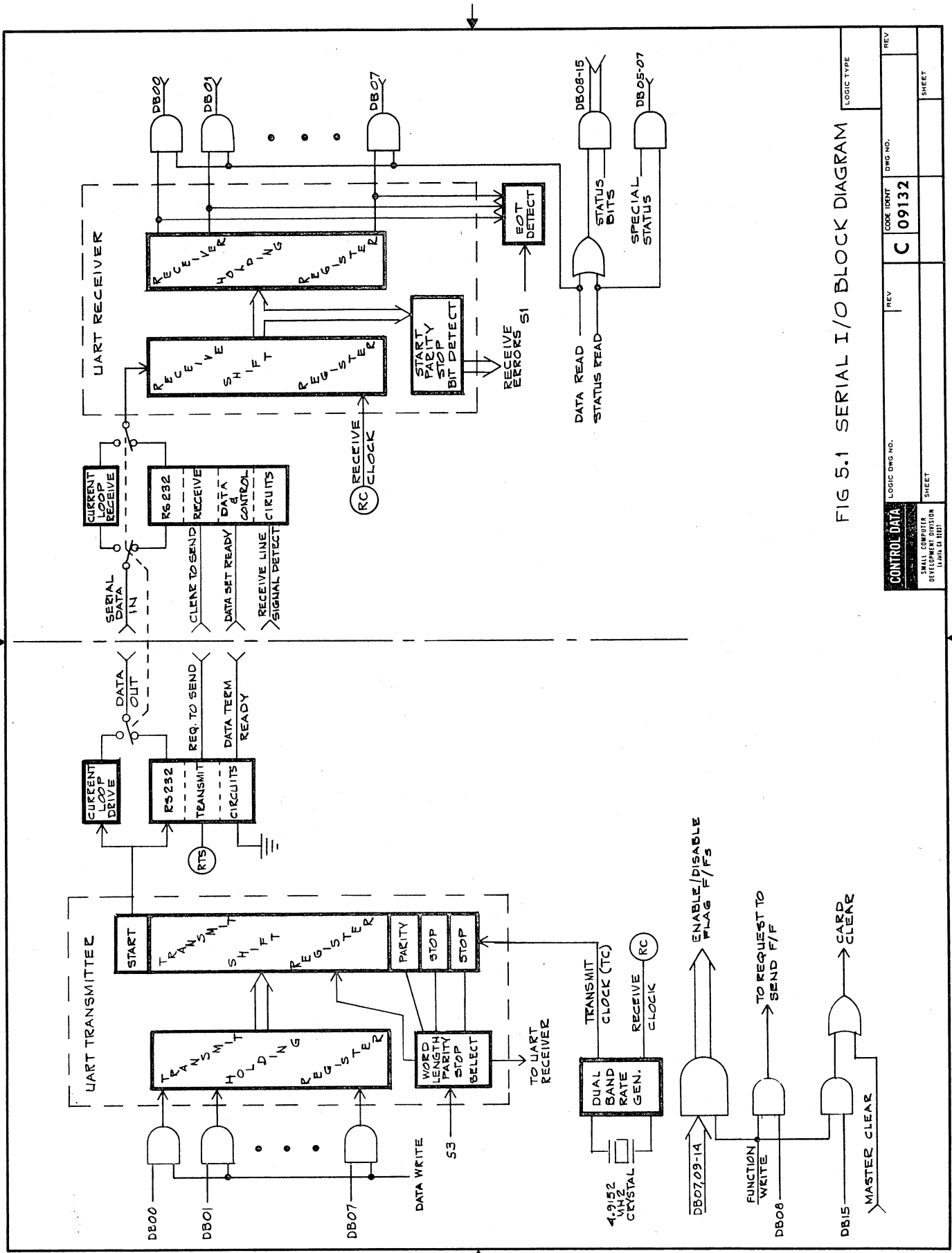
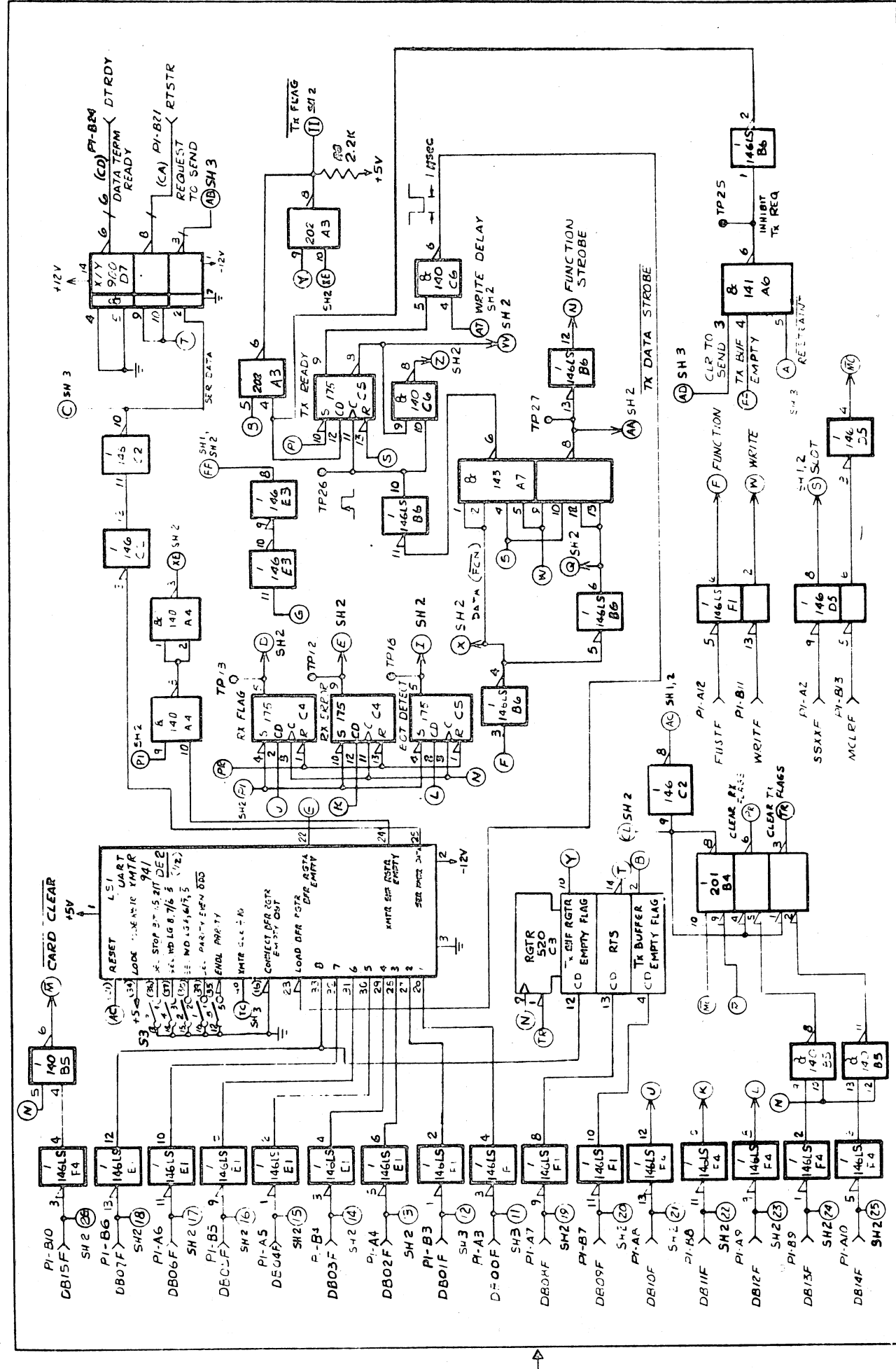


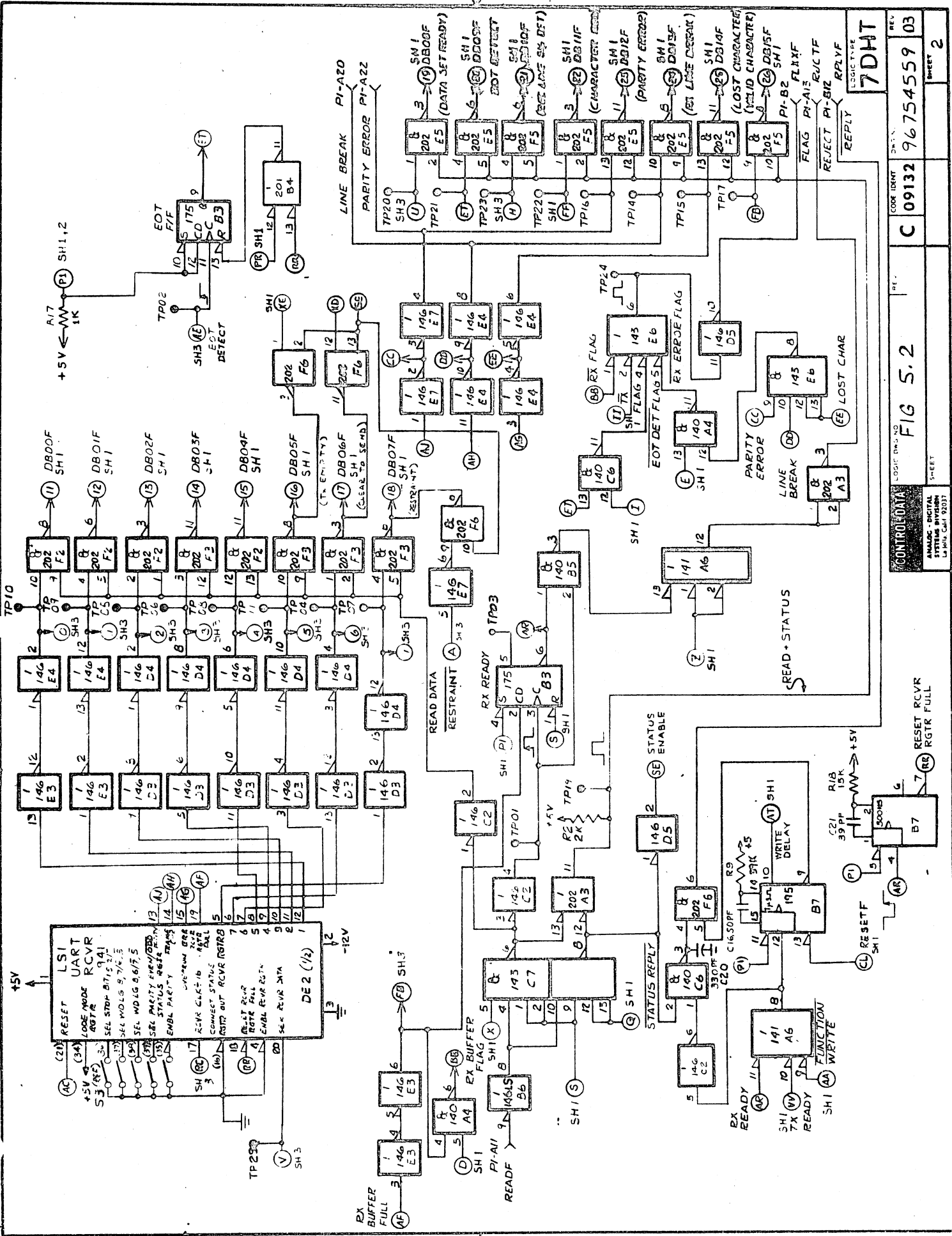
FIG 5.1 SERIAL I/O BLOCK DIAGRAM



**FIG 5.2**

CONTROL DATA	ANALOG DIGITAL SYSTEMS DIVISION	LOGIC DIAGRAM -	DRAWING NUMBER
SERIAL I/O	7DHT	C 09132	9675455903

2. DIODES ARE 25175800.  
 1. DEES ARE IN CIRCUITS AND ARE IDENTIFIED BY THE  
 NOTE WHICH INDICATES THE LOCATION.





SECTION SIX

MAINTENANCE

6.1 PREVENTATIVE MAINTENANCE

No preventative maintenance is required.

6.2 CALIBRATION AND ALIGNMENT

No calibration or alignment is required.

6.3 MAINTENANCE AIDS

Complete access to the components of the serial I/O card requires the use of the ZNMT card extender, CDC part 39844100.

## SECTION SEVEN

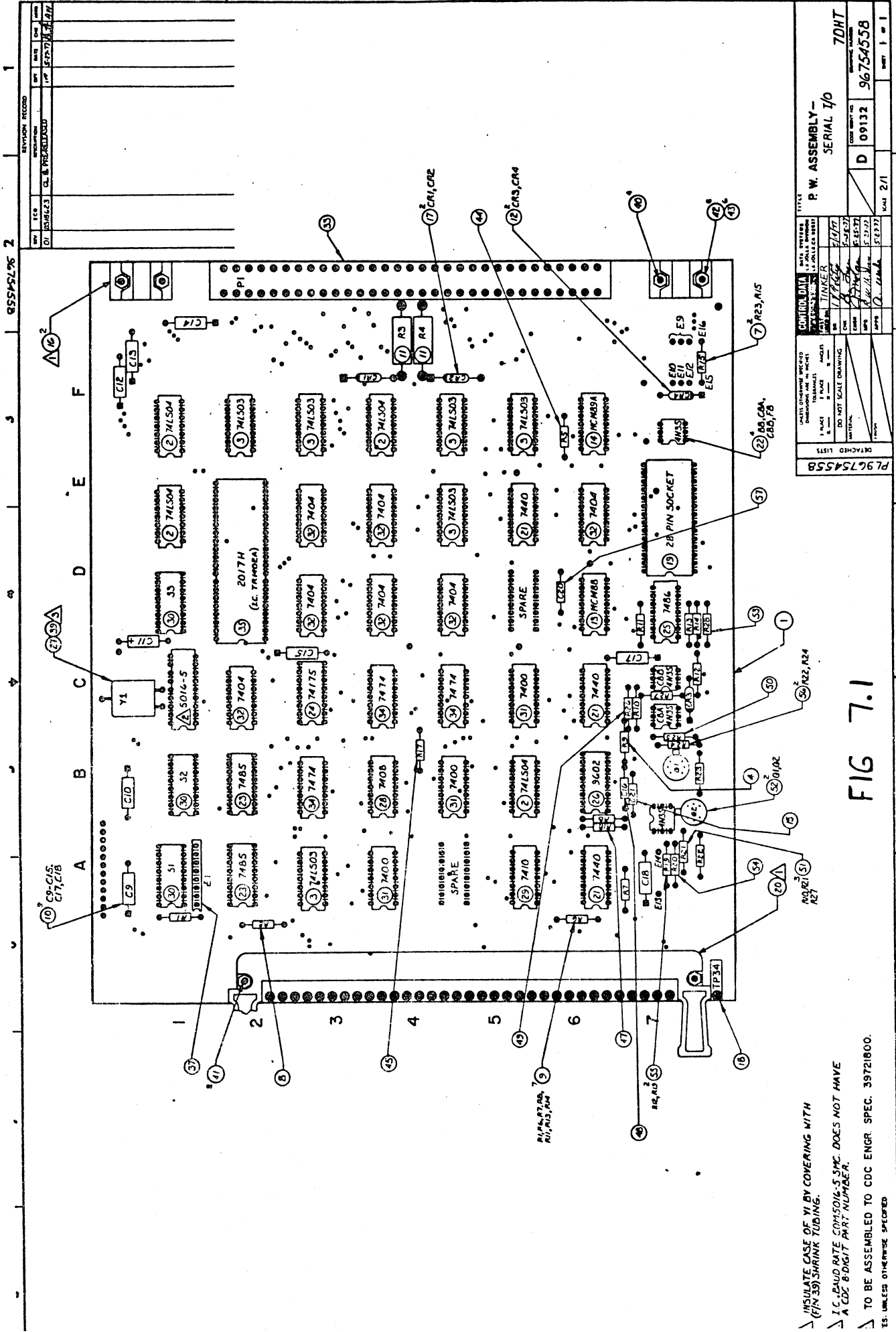
### PARTS DATA

#### 7.1 PRINTED WIRING ASSEMBLY

This section contains the printed wiring assembly for the Serial I/O unit. (Figure 7.1).

#### 7.2 COMPONENT DESCRIPTIONS

This section contains specifications for the UART (Section 7.2.1), the Baud Rate Generator (Section 7.2.2), the RS232 Transmitter (Section 7.2.3), the RS232 Receiver (Section 7.2.4), the current loop transistors (Section 7.2.5) and the Opto-isolator (Section 7.2.6).



REV	ECO	DESCRIPTION	DATE	BY	CHK	APP
01	DA/ML/CS	CL. & PRE-RELEASED	SEP 77	DA/ML/CS		

CONTROL PANEL		PART NUMBER		REV	
P.W. ASSEMBLY		SERIAL 1/0		7DHT	
D 09132		96754558		2/1	
M-137		1-1			

NO.	DESCRIPTION	QTY
1	IC 74LS04	1
2	IC 7404	1
3	IC 7410	1
4	IC 7417	1
5	IC 7400	1
6	IC 7401	1
7	IC 7402	1
8	IC 7403	1
9	IC 7405	1
10	IC 7406	1
11	IC 7407	1
12	IC 7408	1
13	IC 7409	1
14	IC 7411	1
15	IC 7412	1
16	IC 7413	1
17	IC 7414	1
18	IC 7415	1
19	IC 7416	1
20	IC 7418	1
21	IC 7419	1
22	IC 7420	1
23	IC 7421	1
24	IC 7422	1
25	IC 7423	1
26	IC 7424	1
27	IC 7425	1
28	IC 7426	1
29	IC 7427	1
30	IC 7428	1
31	IC 7429	1
32	IC 7430	1
33	IC 7431	1
34	IC 7432	1
35	IC 7433	1
36	IC 7434	1
37	IC 7435	1
38	IC 7436	1
39	IC 7437	1
40	IC 7438	1
41	IC 7439	1
42	IC 7440	1
43	IC 7441	1
44	IC 7442	1
45	IC 7443	1
46	IC 7444	1
47	IC 7445	1
48	IC 7446	1
49	IC 7447	1
50	IC 7448	1
51	IC 7449	1
52	IC 7450	1
53	IC 7451	1
54	IC 7452	1
55	IC 7453	1
56	IC 7454	1
57	IC 7455	1
58	IC 7456	1
59	IC 7457	1
60	IC 7458	1
61	IC 7459	1
62	IC 7460	1
63	IC 7461	1
64	IC 7462	1
65	IC 7463	1
66	IC 7464	1
67	IC 7465	1
68	IC 7466	1
69	IC 7467	1
70	IC 7468	1
71	IC 7469	1
72	IC 7470	1
73	IC 7471	1
74	IC 7472	1
75	IC 7473	1
76	IC 7474	1
77	IC 7475	1
78	IC 7476	1
79	IC 7477	1
80	IC 7478	1
81	IC 7479	1
82	IC 7480	1
83	IC 7481	1
84	IC 7482	1
85	IC 7483	1
86	IC 7484	1
87	IC 7485	1
88	IC 7486	1
89	IC 7487	1
90	IC 7488	1
91	IC 7489	1
92	IC 7490	1
93	IC 7491	1
94	IC 7492	1
95	IC 7493	1
96	IC 7494	1
97	IC 7495	1
98	IC 7496	1
99	IC 7497	1
100	IC 7498	1
101	IC 7499	1
102	IC 7500	1

INSULATE CASE OF Y1 BY COVERING WITH (PIN 39) SHRINK TUBING.

IC BOARD RATE CONSOLE-5 SMC DOES NOT HAVE A CDC BOARD PART NUMBER.

TO BE ASSEMBLED TO CDC ENGR. SPEC. 39721800.

ES UNLESS OTHERWISE SPECIFIED

FIG 7.1

# ASSEMBLY PARTS LIST

MF

SPARE CODE  
S = SPARE PARTS  
N = NON SPARE PARTS

96754558 01 CLB D PWA-SERIAL I/O 7DHT		DS	TINKER	05/25/77	05/25/77	1 / 2
ASSEMBLY DESCRIPTION		DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
DW NUMBER SZ	REV	CLASS	ASSEMBLY DESCRIPTION	QUANTITY	UNIT MEAS.	PART NUMBER
FIND NUMBER SZ	REV	CLASS	ASSEMBLY DESCRIPTION	QUANTITY	UNIT MEAS.	PART NUMBER
43 A	10125800		PC	600	PC	SPRING LOCK WASHERS (MED.)
26 A	15104301		PC	100	PC	IC 9602 MULTIVIB, DUAL RETRIG
35 A	15125700		PC	100	PC	I.C. TRI402A UNIV. ASYNCHRON.
2 A	15145100		PC	400	PC	IC TTL HEX INVERTER 74LS04
3 A	15145200		PC	600	PC	IC TTL QUAD 2INPUT NAND 74LS03
4 C	17705902		PC	100	PC	RES FXD .25W 39000 OHMS
51 C	17705905		PC	300	PC	RES FXD .25W 51000 OHMS
50 C	24500041		PC	100	PC	RES FXD .25W 120 OHMS
49 C	24500049		PC	100	PC	RES FXD .25W 270 OHMS
55 C	24500052		PC	200	PC	RES FXD .25W 360 OHMS
56 C	24500055		PC	200	PC	RES FXD .25W 470 OHMS
7 C	24500056		PC	200	PC	RES FXD .25W 510 OHMS
45 C	24500063		PC	100	PC	RES FXD .25W 1000 OHMS
8 C	24500070		PC	100	PC	RES FXD .25W 2000 OHMS
9 C	24500071		PC	700	PC	RES FXD .25W 2200 OHMS
44 C	24500080		PC	100	PC	RES FXD .25W 5100 OHMS
53 C	24500081		PC	100	PC	RES FXD .25W 5600 OHMS
54 C	24500087		PC	100	PC	RES FXD .25W 10000 OHMS
47 C	24500091		PC	100	PC	RES FXD .25W 15000
10 C	24505229		PC	900	PC	CAP, FXD SOL TA 35V 1.0UF 10PCT
11 A	24507121		PC	200	PC	RES-FXD COMP. 68 OHM IH. 5 PCT
12 A	25175800		PC	200	PC	DIODE (1N914)
39 A	25196908		IN	100	IN	INSUL SLEEVE SHRINK 3/4 CLEAR
13 A	36186400		PC	100	PC	IC CHIP, TYPE 1488
14 A	36186501		PC	100	PC	IC CHIP TYPE 1489
52 A	38838800		PC	200	PC	TRANSISTOR- 2N2223, NPN, SIL
18 A	38958502		PC	100	PC	TEST JACK, BLACK
17 A	39547100		PC	200	PC	DIODE ZENER 12V
16 C	39827500		PC	200	PC	GUIDE, APPROACH
19 A	51858101		PC	100	PC	SOCKET, IC, PC AND WIRE WRAP 28P
20 D	52936000		PC	100	PC	AIR SEAL - 25 PAK
21 A	66299102		PC	300	PC	IC TTL DVAL 4-IN NAND
22 C	72313600		PC	400	PC	PHOTO TRANSISTOR OPTO-ISOLAOR
15 A	84996706		PC	100	PC	CAP, CER 100V 39 PF
48 A	84996708		PC	100	PC	CAP, CER 100V 50 PF
57 A	84996719		PC	100	PC	CAP, CER 100V 330 PF

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### Subsection 7.2.1

#### Universal Asynchronous

#### Receiver Transmitter (UART)

Either the Western Digital TR1602 or the Standard Microsystems Corp. COM2017/H may be supplied as the UART for the DK611-A. The two devices are pin compatible and differ in operation in only one area. Master Reset will clear the receive holding register on the TR1602. The 2017 does not clear the register with Master Reset applied. However, the logic has been designed to operate with either UART.

**FEATURES**

- **SILICON GATE TECHNOLOGY – LOW THRESHOLD CIRCUITRY**  
Directly TTL and DTL Compatible – External Resistors Eliminated
- **D. C. STABLE (STATIC) CIRCUITRY**
- **FULL DUPLEX OR HALF DUPLEX OPERATION**  
Transmits And Receives Serial Data Simultaneously Or Alternately
- **AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK**
- **AUTOMATIC START BIT GENERATION**
- **BUFFERED RECEIVER AND TRANSMITTER REGISTERS**
- **FULLY PROGRAMMABLE – EXTERNALLY SELECTABLE**  
Word Length  
Baud Rate  
Even/Odd Parity (Receiver/Verification – Transmitter/Generation)  
Parity Inhibit – Verification/Generation  
One, One and One-Half, or Two Stop Bit Generation
- **AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION**  
Transmission Complete                      Parity Error  
Buffer Register Transfer Complete        Framing Error  
Received Data Available                      Overrun Error
- **THREE-STATE OUTPUTS**  
Receiver Register Outputs  
Status Flags
- **AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES**

**APPLICATIONS**

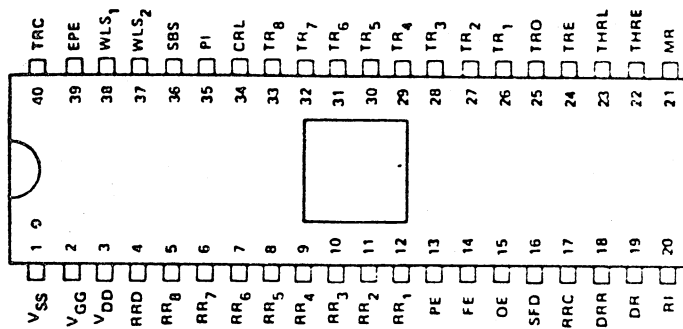
- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

**GENERAL DESCRIPTION**

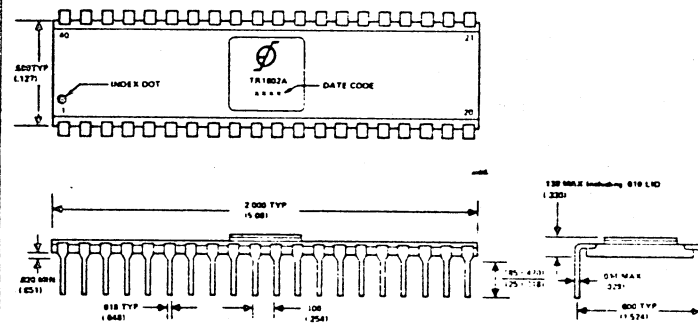
The TR1602A & the TR1602B are ASYNCHRONOUS RECEIVER/TRANSMITTER sub-systems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. Note: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

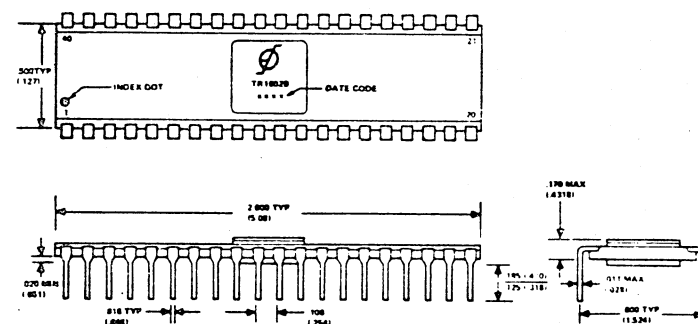
**PIN CONNECTIONS**



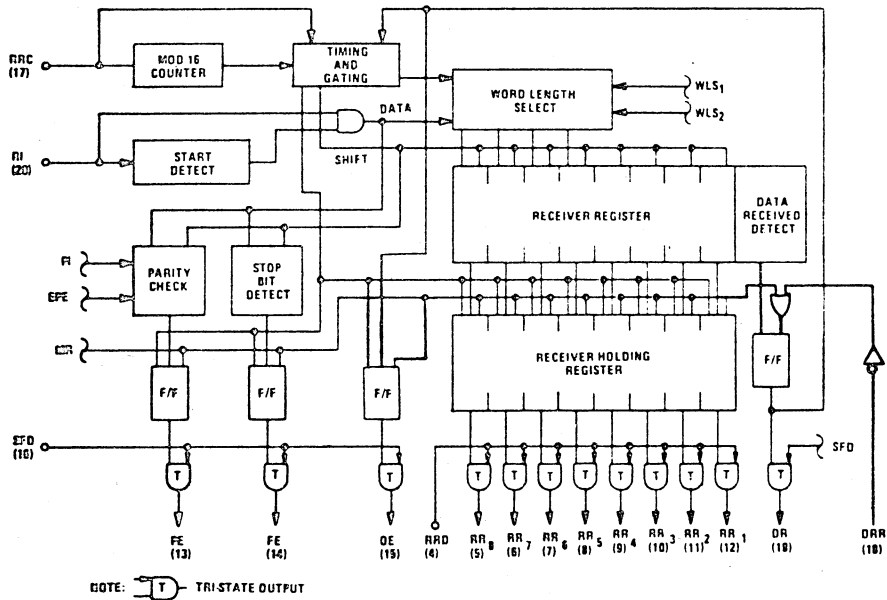
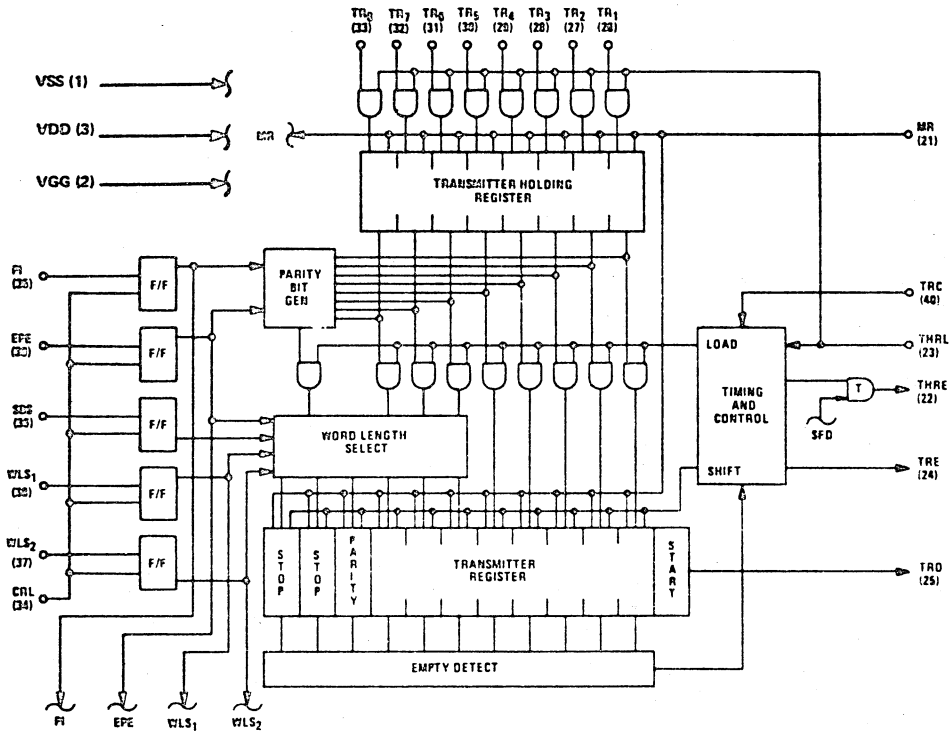
**TR1602A CERAMIC PACKAGE OUTLINE**



**TR1602B HERMETIC PLASTIC CAVITY PACKAGE OUTLINE**



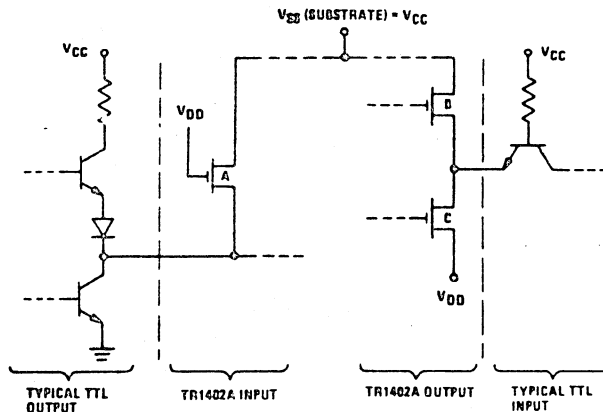




NOTE: TRI-STATE OUTPUT

### INPUT STRUCTURE

MOS DEVICE "A" ACTS AS AN INTERNAL PULL-UP RESISTOR TO  $V_{SS} = V_{CC}$  WHICH BIASES OFF THE CASCODE DEVICE OF THE TTL OUTPUT IN THE HIGH-LEVEL OUTPUT STATE. IN THE LOW-LEVEL OUTPUT STATE THE TTL OUTPUT DEVICE SINKS THE CURRENT SUPPLIED BY DEVICE "A".



### OUTPUT STRUCTURE

DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.



## PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V <sub>SS</sub> Power Supply	V <sub>SS</sub>	+5 volts supply
2	V <sub>GG</sub> Power Supply	V <sub>GG</sub>	-12 volts supply
3	V <sub>DD</sub> Power Supply	V <sub>DD</sub>	Ground
4	Receiver Register Disconnect	RRD	A high level input voltage, V <sub>IH</sub> , applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR <sub>8</sub> -RR <sub>1</sub> data outputs (pins 5-12).
5-12	Receiver Holding Register Data	RR <sub>8</sub> - RR <sub>1</sub>	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V <sub>IL</sub> , is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR <sub>1</sub> (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V <sub>OL</sub> .
13	Parity Error	PE	A high level output voltage, V <sub>OH</sub> , on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	Framing Error	FE	A high-level output voltage, V <sub>OH</sub> , on this line indicates that the received character has no valid stop bit, ie., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	Overflow Error	OE	A high-level output voltage, V <sub>OH</sub> , on this line indicates that the Data REceived Flag (pin 19) was not reset before the next character was transferred to the REceiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	Status Flags Disconnect	SFD	A high-level input voltage, V <sub>IH</sub> , applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	Data Received Reset	DRR	A low-level input voltage, V <sub>IL</sub> , applied to this line resets the DR line.
19	Data Received	DR	A high-level output voltage, V <sub>OH</sub> , indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V <sub>IH</sub> , must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high-level input voltage, V <sub>IH</sub> , to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V <sub>OH</sub> .
22	Transmitter Holding Register Empty	THRE	A high-level output Voltage, V <sub>OH</sub> , on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

## PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION															
23	Transmitter Holding Register Load	THRL	A low-level input voltage, $V_{IL}$ , applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, $V_{IL}$ , to a high-level input voltage, $V_{IH}$ , transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.															
24	Transmitter Register Empty	TRE	A high-level output voltage, $V_{OH}$ , on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.															
25	Transmitter Register Output	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, $V_{OH}$ . Start of transmission is defined as the transition of the START bit from a high-level output voltage, $V_{OH}$ , to a low-level output voltage, $V_{OL}$ .															
26-33	Transmitter Register Data Inputs	TR <sub>1</sub> - TR <sub>8</sub>	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS <sub>1</sub> and WLS <sub>2</sub> ), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, $V_{IH}$ , will cause a high-level output voltage, $V_{OH}$ , to be transmitted.															
34	Control Register Load	CRL	A high-level input voltage, $V_{IH}$ , on this line loads the CONTROL REGISTER with the control bits (WLS <sub>1</sub> , WLS <sub>2</sub> , EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, $V_{IH}$ .															
35	Parity Inhibit	PI	A high-level input voltage, $V_{IH}$ , on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to $V_{OL}$ . If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.															
36	Stop Bit(s) Select	SBS	This line selects the number of STOP bits to be transmitted after the PARITY bit. A high-level input voltage, $V_{IH}$ , on this line selects two STOP bits, and a low-level input voltage, $V_{IL}$ , selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.															
37-38	Word Length Select	WLS <sub>2</sub> - WLS <sub>1</sub>	<p>These two lines select the character length (exclusive of parity) as follows:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">WLS<sub>2</sub></th> <th style="text-align: center;">WLS<sub>1</sub></th> <th style="text-align: center;">Word Length</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;"><math>V_{IL}</math></td> <td style="text-align: center;"><math>V_{IL}</math></td> <td style="text-align: center;">5 bits</td> </tr> <tr> <td style="text-align: center;"><math>V_{IL}</math></td> <td style="text-align: center;"><math>V_{IH}</math></td> <td style="text-align: center;">6 bits</td> </tr> <tr> <td style="text-align: center;"><math>V_{IH}</math></td> <td style="text-align: center;"><math>V_{IL}</math></td> <td style="text-align: center;">7 bits</td> </tr> <tr> <td style="text-align: center;"><math>V_{IH}</math></td> <td style="text-align: center;"><math>V_{IH}</math></td> <td style="text-align: center;">8 bits</td> </tr> </tbody> </table>	WLS <sub>2</sub>	WLS <sub>1</sub>	Word Length	$V_{IL}$	$V_{IL}$	5 bits	$V_{IL}$	$V_{IH}$	6 bits	$V_{IH}$	$V_{IL}$	7 bits	$V_{IH}$	$V_{IH}$	8 bits
WLS <sub>2</sub>	WLS <sub>1</sub>	Word Length																
$V_{IL}$	$V_{IL}$	5 bits																
$V_{IL}$	$V_{IH}$	6 bits																
$V_{IH}$	$V_{IL}$	7 bits																
$V_{IH}$	$V_{IH}$	8 bits																
39	Even Parity Enable	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, $V_{IH}$ , selects even PARITY and a low-level input voltage, $V_{IL}$ , selects odd PARITY.															
40	Transmitter Register Clock	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.															

## MAXIMUM RATINGS

$V_{GG}$ Supply Voltage	+0.3V to - 20V
$V_{DD}$ Supply Voltage	+0.3V to - 20V
Clock Input Voltage*	+0.3V to - 20V
Logic Input Voltage*	+0.3V to - 20V
Logic Output Voltage*	+0.3V to - 20V
Storage Temperature	-55°C to +150°C
Operating Free-Air Temperature $T_A$ Range	0°C to + 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

\* $V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to  $V_{SS}$  (Substrate)

## ELECTRICAL CHARACTERISTICS

( $V_{SS} = V_{CC} = 5V \pm 5\%$ ,  $V_{DD} = 0V$ ,  $V_{GG} = -12V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$  unless otherwise specified)

SYM	PARAMETER	MIN	MAX	CONDITIONS
$I_{SS}$	OPERATING CURRENT			
	Substrate Supply Current		24 ma	$V_{SS} = 5.25V$ , $V_{IN} = OPEN$
	Substrate Supply Current		60 ma	$V_{SS} = 5.25V$ , $V_{IN} = +0.4V$
$I_{GG}$	Gate Supply Current		6 ma	
	LOGIC LEVELS			
$V_{IH}$	Logic High	$V_{SS} - 1.5V$		
$V_{IL}$	Logic Low		0.8 V	$V_{SS} = 4.75V$
	OUTPUT LOGIC LEVELS			
$V_{OH}$	Logic High	$V_{SS} - 1.0V$		$V_{SS} = 4.75V$ , $I_{OH} = -100\mu a$
$V_{OL}$	Logic Low		0.4 V	$V_{SS} = 5.25V$ , $I_{OL} = 1.6 ma$
$I_{OS}^*$	Short Circuit Current		-2.2 ma	$V_{SS} = 5.25V$ , $V_O = 0V$
$I_{OC}$	Output Leakage		10 $\mu a$	$V_{OUT} = 0V$ , $SFD=RRD=V_{IH}$
$I_{IL}$	Low Level Input Current		-1.6 ma	$V_{SS} = 5.25$ , $V_{IN} = 0.4V$

\*Only one output should be shorted at any time.

# SWITCHING CHARACTERISTICS - See "Switching Waveforms"

( $V_{SS} = V_{CC} = 5V$ ,  $V_{DD} = 0V$ ,  $V_{GG} = -12V$ ,  $T_A = 25^\circ$ ,  $C_{LOAD} = 20$  pf plus one TTL load)

SYM	PARAMETER	MIN	MAX	CONDITIONS
$f_{clock}$	Clock Frequency	D.C.	320kHz*	$V_{SS} = 4.75V$ (See figures 1 & 2)
$t_{pw}$	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
$t_c$	Coincidence Time	200 ns		(See figure 1 & 2)
$t_{hold}$	Hold Time	20 ns		(See figure 1 & 2)
$t_{set}$	Set Time	0		(See figure 1 & 2)
	Output Propagation Delays			
$t_{pd0}$	To Low State		500 ns	(See figure 3) $C_L = 20$ pf, plus one TTL load
$t_{pd1}$	To High State		500 ns	(See figure 3) $C_L = 20$ pf, plus one TTL load
	Capacitance			
$C_{in}$	Inputs		20 pf	$f = 1$ MHz, $V_{in} = 5V$
$C_o$	Outputs		20 pf	$f = 1$ MHz, $V_{in} = 5V$

- \* $f_{max}$  for TR1602A or B      320kHz
- $f_{max}$  for TR1602A or B-03    480kHz
- $f_{max}$  for TR1602A or B-04    640kHz
- $f_{max}$  for TR1602A or B-05    800kHz

## SWITCHING WAVE FORMS

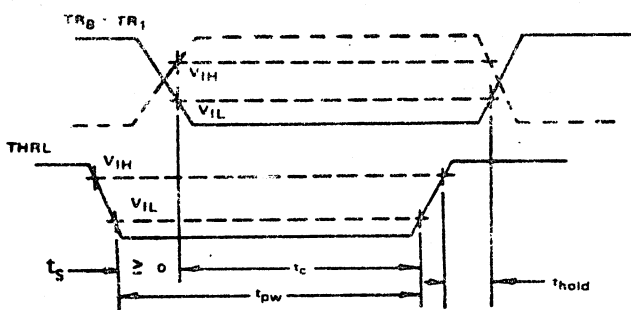


FIGURE 1. DATA INPUT LOAD CYCLE

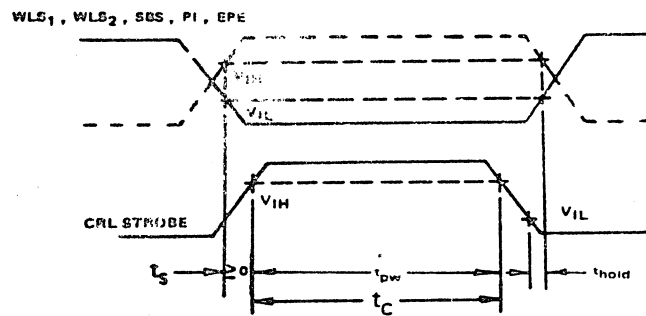
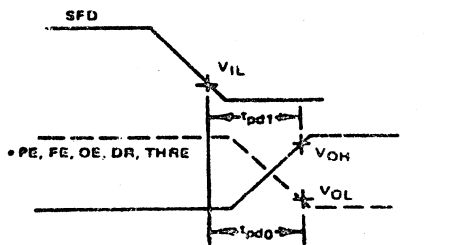
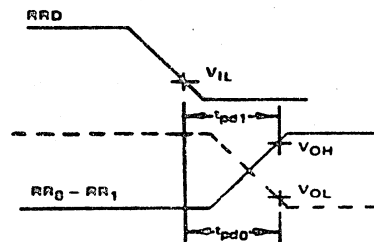


FIGURE 2. CONTROL REGISTER LOAD CYCLE



\* OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM  $V_{IL}$  TO  $V_{IH}$

FIGURE 3. STATUS FLAG OUTPUT DELAYS



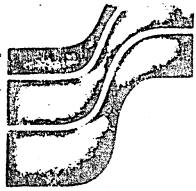
\*  $RR_0 - RR_1$  ARE DISCONNECTED AT TRANSITION OF RRD FROM  $V_{IL}$  TO  $V_{IH}$

FIGURE 4. DATA OUTPUT DELAYS

## Subsection 7.2.2

### Dual Baud Rate Generator

The following subsection is a reprint of the Standard Microsystems Corp's COM5016 series specification. Although the reprint covers three separate units, only the 5016-5 is used on the DK611-A.



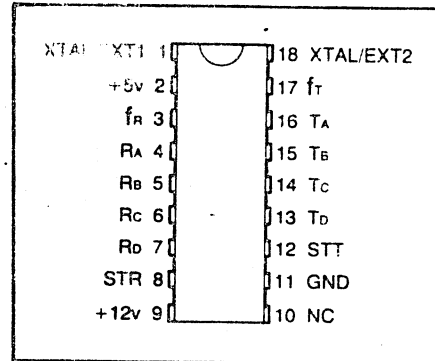
# Dual Baud Rate Generator

## Programmable Divider

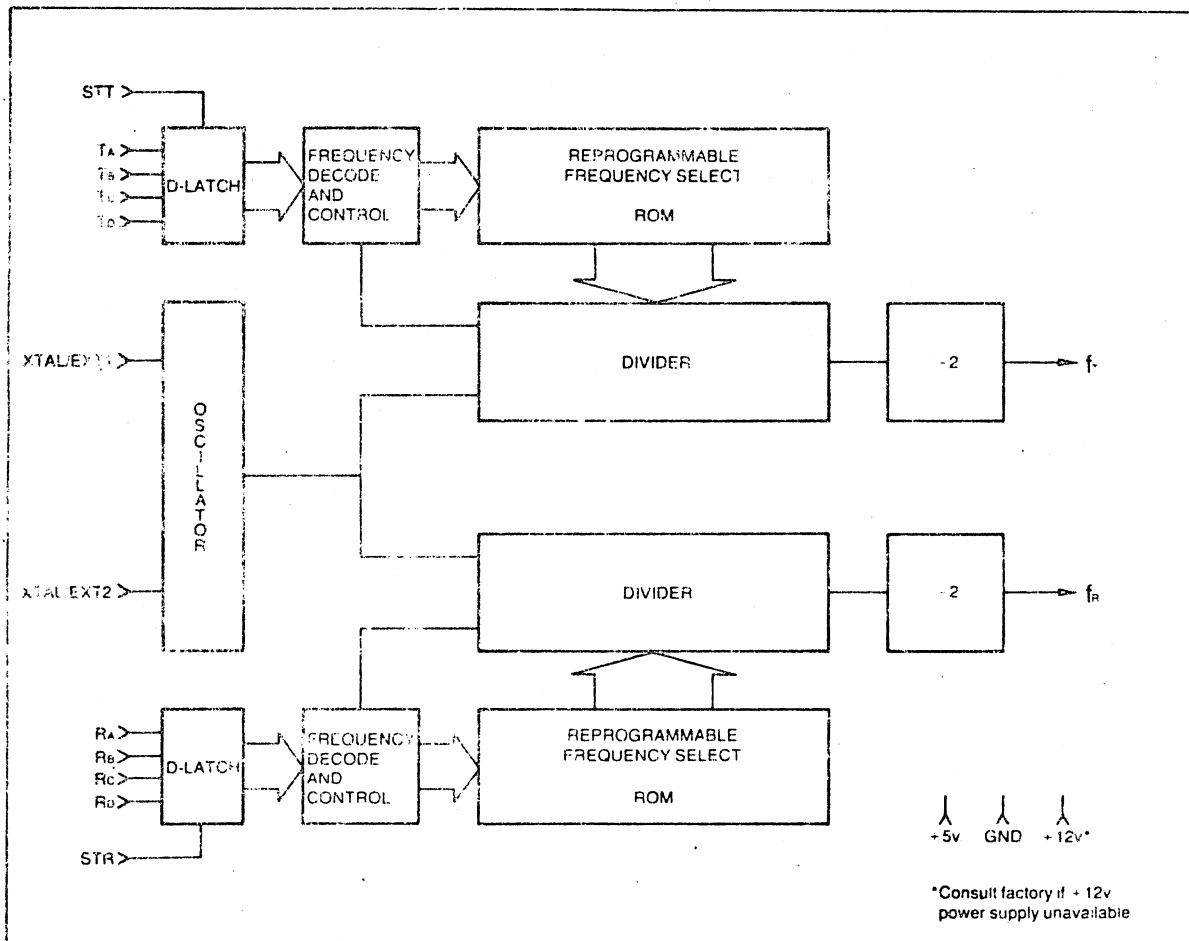
### FEATURES

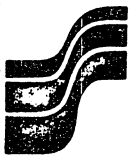
- On chip crystal oscillator or external frequency input
- Choice of 2 X 16 output frequencies
- 16 asynchronous/synchronous baud rates
- Direct UART/USRT compatibility
- Full duplex communication capability
- Re-programmable ROM allows generation of other frequencies
- TTL, MOS compatibility
- On chip input pull-up resistors
- 0.01% accuracy—typical
- 50% Duty Cycle
- 18 pin ceramic DIP package

### PIN CONFIGURATION



### BLOCK DIAGRAM





## General Description

The Standard Microsystems COM 5016 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS<sup>®</sup> MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, or each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to  $(2^{15} - 1)$ .

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016 can be driven by either an external crystal or TTL logic level inputs; COM 5016T is driven by TTL logic level inputs only.

### MAXIMUM GUARANTEED RATINGS\*

Operating Temperature Range	.....	0°C to + 70°C
Storage Temperature Range	.....	-55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	.....	+325°C
Positive Voltage on any Pin, with respect to ground	.....	+18.0V
Negative Voltage on any Pin, with respect to ground	.....	-0.3V

\*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=0°C to 70°C, V<sub>CC</sub>=+5V±5%, V<sub>DD</sub>=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max	Unit	Comments
<b>D.C. CHARACTERISTICS</b>					
<b>INPUT VOLTAGE LEVELS</b>					
Low-level, V <sub>IL</sub>			0.8	V	excluding XTAL inputs
High-level, V <sub>IH</sub>	V <sub>CC</sub> -1.5		V <sub>CC</sub>	V	
<b>OUTPUT VOLTAGE LEVELS</b>					
Low-level, V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 3.2mA
High-level, V <sub>OH</sub>	V <sub>CC</sub> -1.5	4.0		V	I <sub>OH</sub> = 100µA
<b>INPUT CURRENT</b>					
Low-level, I <sub>IL</sub>			0.3	mA	V <sub>IN</sub> = GND, excluding XTAL input
<b>INPUT CAPACITANCE</b>					
All inputs, C <sub>IN</sub>		5	10	pf	V <sub>IN</sub> = GND, excluding XTAL input
<b>EXT INPUT LOAD</b>					
		8	10		Series 7400 unit loads
<b>POWER SUPPLY CURRENT</b>					
I <sub>CC</sub>		28	45	mA	
I <sub>DD</sub>		12	22	mA	
<b>A.C. CHARACTERISTICS</b>					
CLOCK FREQUENCY		5.0688		MHz	T <sub>A</sub> = +25°C XTAL, EXT
<b>PULSE WIDTH</b>					
Clock					50% Duty Cycle ±5%
Receiver strobe	150		DC	ns	See Note 1.
Transmitter strobe	150		DC	ns	See Note 1.
<b>INPUT SET-UP TIME</b>					
Address	50			ns	See Note 1.
<b>INPUT HOLD TIME</b>					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY		2.0	2.5	µs	=1/f <sub>IN</sub> (12)

Note 1: Input set-up time can be decreased to ≥ 0ns by increasing the minimum strobe width by 50ns to a total of 200ns.

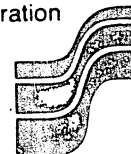
**Table 1.**

**CRYSTAL FREQUENCY = 5.0688 MHz**

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

**Description of Pin Functions**

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V <sub>CC</sub>	Power Supply	+5 volt Supply
3	f <sub>R</sub>	Receiver Output Frequency	This output runs at a frequency as selected by the Receiver Address.
4-7	R <sub>A</sub> , R <sub>B</sub> , R <sub>C</sub> , R <sub>D</sub>	Receiver Address	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f <sub>R</sub> .
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R <sub>A</sub> , R <sub>B</sub> , R <sub>C</sub> , R <sub>D</sub> ) into the receiver address register. This input may be strobed or hard wired to a high-level.
9	V <sub>DD</sub>	Power Supply	+12 volt Supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T <sub>A</sub> , T <sub>B</sub> , T <sub>C</sub> , T <sub>D</sub> ) into the transmitter address register. This input may be strobed or hard wired to a high-level.
13-16	T <sub>D</sub> , T <sub>C</sub> , T <sub>B</sub> , T <sub>A</sub>	Transmitter Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f <sub>T</sub> .
17	f <sub>T</sub>	Transmitter Output Frequency	This output runs at a frequency as selected by the Transmitter Address.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.



**Table 2.**  
**COM 5016-5**

CRYSTAL FREQUENCY = 4.9152 MHz

Transmit/Receive Address				Baud Rate	Theoretical Frequency		Actual Frequency		Percent Error	Duty Cycle %	Divisor
D	C	B	A		16X Clock	16X Clock	16X Clock	16X Clock			
0	0	0	0	50	0.8	KHz	0.8	KHz	—	50/50	6144
0	0	0	1	75	1.2		1.2		—	50/50	4096
0	0	1	0	110	1.76		1.7598		-0.01	*	2793
0	0	1	1	134.5	2.152		2.152		—	50/50	2284
0	1	0	0	150	2.4		2.4		—	50/50	2048
0	1	0	1	300	4.8		4.8		—	50/50	1024
0	1	1	0	600	9.6		9.6		—	50/50	512
0	1	1	1	1200	19.2		19.2		—	50/50	256
1	0	0	0	1800	28.8		28.7438		-0.19	*	171
1	0	0	1	2000	32.0		31.9168		-0.26	50/50	154
1	0	1	0	2400	38.4		38.4		—	50/50	128
1	0	1	1	3600	57.6		57.8258		0.39	*	85
1	1	0	0	4800	76.8		76.8		—	50/50	64
1	1	0	1	7200	115.2		114.306		-0.77	*	43
1	1	1	0	9600	153.6		153.6		—	50/50	32
1	1	1	1	19,200	307.2		307.2		—	50/50	16

\*When the duty cycle is not exactly 50% it is 50% ± 10%

**Table 3.**  
**COM 5016-6**  
**COM 5016T-6**

CRYSTAL FREQUENCY = 5.0688 MHz

Transmit/Receive Address				Baud Rate	Theoretical Frequency		Actual Frequency		Percent Error	Duty Cycle %	Divisor
D	C	B	A		32X Clock	32X Clock	32X Clock	32X Clock			
0	0	0	0	50	1.6	KHz	1.6	KHz	—	50/50	3168
0	0	0	1	75	2.4		2.4		—	50/50	2112
0	0	1	0	110	3.52		3.52		—	50/50	1440
0	0	1	1	134.5	4.304		4.303		.026	50/50	1178
0	1	0	0	150	4.8		4.8		—	50/50	1056
0	1	0	1	200	6.4		6.4		—	50/50	792
0	1	1	0	300	9.6		9.6		—	50/50	528
0	1	1	1	600	19.2		19.2		—	50/50	264
1	0	0	0	1200	38.4		38.4		—	50/50	132
1	0	0	1	1800	57.6		57.6		—	50/50	88
1	0	1	0	2400	76.8		76.8		—	50/50	66
1	0	1	1	3600	115.2		115.2		—	50/50	44
1	1	0	0	4800	153.6		153.6		—	*	33
1	1	0	1	7200	230.4		230.4		—	50/50	22
1	1	1	0	9600	307.2		298.16		2.941	*	17
1	1	1	1	19,200	614.4		633.6		3.125	50/50	8

\*When the duty cycle is not exactly 50% it is 50% ± 10%

### Subsection 7.2.3

#### RS232-C Transmitter

The specifications for a quad RS232 transmit integrated circuit - the 1488 - are included in this subsection. This device has multiple sources such as Harris Semiconductor (HD1488), Motorola (MC1488) Texas Instruments (75188) . . . etc. The specification included is from the Harris HD 1488.



**HARRIS**  
SEMICONDUCTOR  
A DIVISION OF HARRIS CORPORATION

# HD-1488

## Quad Line Driver

### FEATURES

- $\pm 6.0V$  OUTPUT LEVELS
- SHORT CIRCUIT PROTECTED
- USEFUL AS LOGIC LEVEL SHIFTER
- MONOLITHIC RELIABILITY

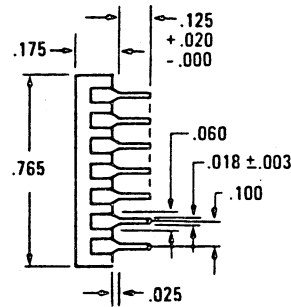
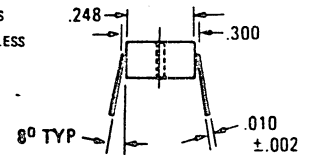
### DESCRIPTION

The Harris HD-1488 is a quadruple line driver monolithic integrated circuit meeting the electrical requirements of EIA standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The driver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit inputs can be driven from any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line receiver circuit is the Harris HD-1489.

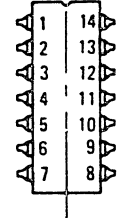
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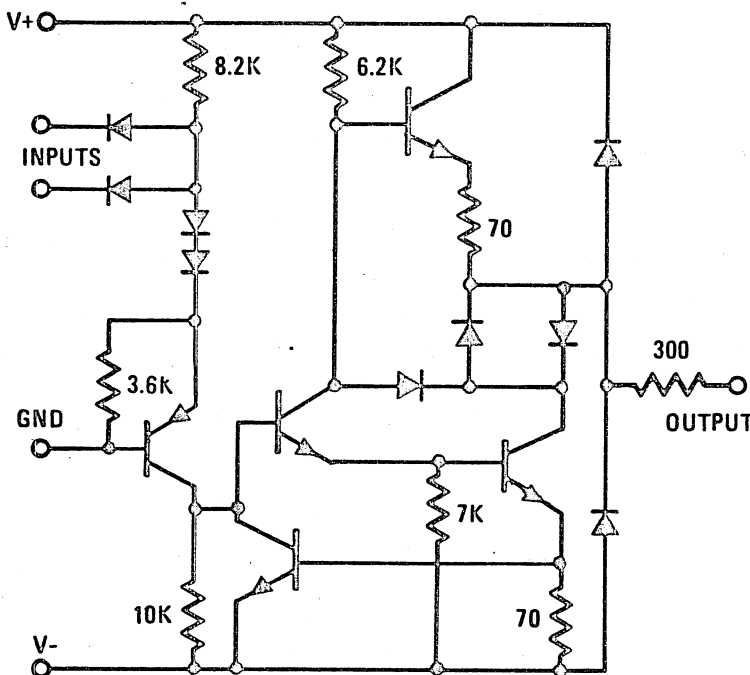
ALL DIMENSIONS IN INCHES  
ALL DIMENSIONS  $\pm .010$  UNLESS  
OTHERWISE SHOWN.



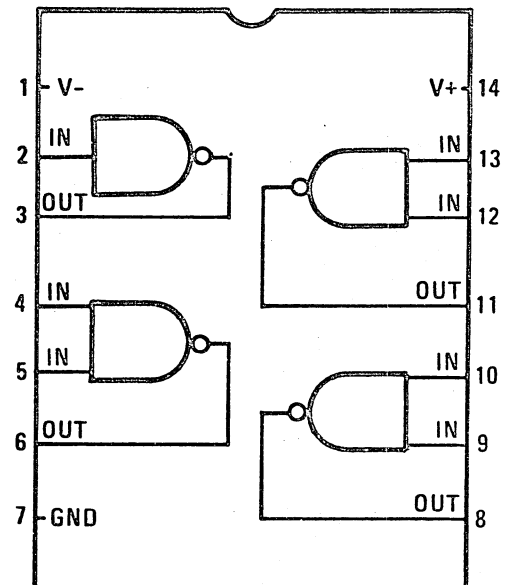
INDEX NOTCH



### SCHEMATIC



### CONNECTION DIAGRAM



# SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+, V- at +25°C Derate by 35mV/°C	±15.0V	Storage Temperature	-65°C to +150°C
Input Voltage	$V- \leq V_{IN} \leq 7.0V$	Operating Temperature, T <sub>A</sub>	0°C to +75°C
Output Voltage	$V_{OUT} \geq V+ +5V$ $\leq V- -5V$	Power Dissipation at +25°C Derate by 6.7mW/°C	1000mW

## ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = +9.0V, V- = -9.0V, T<sub>A</sub> = 0°C to +75°C unless otherwise specified.

PARAMETER	SYM.	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
Input Current	"0"	I <sub>F</sub>		1.0	1.3	mA	V <sub>IN</sub> = 0.0V
	"1"	I <sub>R</sub>			10	μA	V <sub>IN</sub> = +5.0V
Output Voltage	"0"	V <sub>OL</sub>	-6.0	-7.0		V	V <sub>IN</sub> = +1.9V, R <sub>L</sub> = 3K
	"1"	V <sub>OH</sub>	+6.0	+7.0			V <sub>IN</sub> = +0.8V, R <sub>L</sub> = 3K
Output Short Circuit Current	I <sub>SC+</sub>		+6	+10	+12	mA	V <sub>IN</sub> = 0.0V to +0.8V
	I <sub>SC-</sub>		-6	-10	-12		V <sub>IN</sub> = +1.9V to ±5.0V
D.C. Output Resistance	R <sub>O</sub>	300				Ohms	V+ = V- = 0.0V V <sub>O</sub> = ±2.0V
Supply Current	I+			+15	+20	mA	V+ = +9.0V
	I-			-13	-17		V- = -9.0V
	I+			+19	+25	mA	V+ = +12.0V
	I-			-18	-23		V- = -12.0V
Power Dissipation	P <sub>D</sub>				333	mW	V+ = +9.0V, V- = -9.0V
	P <sub>D</sub>				576		V+ = +12.0V, V- = -12.0V
A.C. Propagation Delay	T <sub>PD+</sub>			250	300	ns	R <sub>L</sub> = 3KΩ
	T <sub>PD-</sub>			30	120		
	Rise Time (Note 1)	T <sub>r</sub>		50	100	ns	C <sub>L</sub> = 15pF
Fall Time (Note 1)	T <sub>f</sub>		25	75	ns	T <sub>A</sub> = +25°C	

NOTES: 1. To maintain a maximum rate of voltage change of 30V/μs, the load capacitance, including transmission line, should be at least 330pF.

#### Subsection 7.2.4

#### RS232-C Receiver

This subsection includes the specifications of the quad RS232 receiver - the 1489A - used in the DK611-A. The specification is for the Texas Instruments 75189/89A although the Harris HD1489 and Motorola MC1489 are equivalent. Note that by connecting pin 12 to +5 volts through a 5K resistor provides the data circuit with a fail safe indication if the line opens or shorts to ground.

# TYPES SN75189, SN75189A QUADRUPLE LINE RECEIVERS

electrical characteristics over operating free-air temperature range,  $V_{CC} = 5V \pm 1\%$ , (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SN75189			SN75189A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{T+}$ Positive-going threshold voltage	1		1	1.5		1.75	1.9		V
$V_{T-}$ Negative-going threshold voltage	1		0.75	1.25		0.75	0.97		V
$V_{OH}$ High-level output voltage	1	$V_I = 0.75V$ , $I_{OH} = -0.5mA$	2.6	4	5	2.6	4		V
		Input open, $I_{OH} = -0.5mA$	2.6	4	5	2.6	4		V
$V_{OL}$ Low-level output voltage	1	$V_I = 3V$ , $I_{OL} = 10mA$		0.2	0.45		0.2	0.45	V
$I_{IH}$ High-level input current	2	$V_I = 25V$	3.6		8.3	3.6		8.3	mA
		$V_I = 3V$	0.43			0.43			mA
$I_{IL}$ Low-level input current	2	$V_I = -25V$	-3.6		-8.3	-3.6		-8.3	mA
		$V_I = -3V$	-0.43			-0.43			mA
$I_{OS}$ Short-circuit output current	3			-3			-3		mA
$I_{CC}$ Supply current	2	$V_I = 5V$ , Outputs open		20	26		20	26	mA

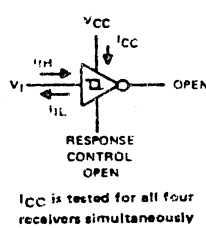
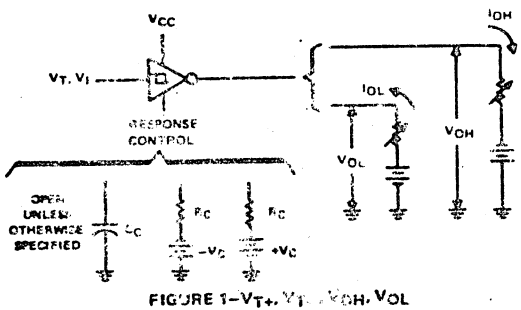
†All characteristics are measured with the response control terminal open.

‡All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

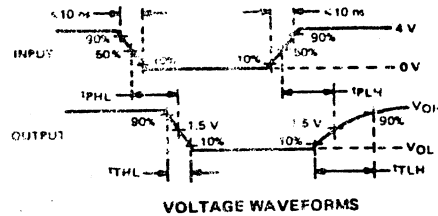
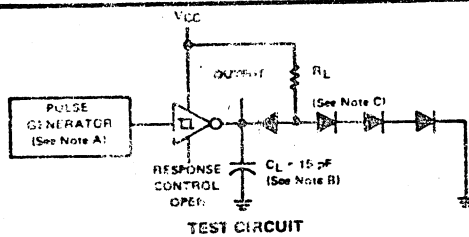
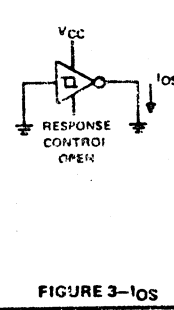
switching characteristics,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ Propagation delay time, low-to-high-level output	4	$C_L = 15pF$ , $R_L = 3.9k\Omega$		25	85	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output		$C_L = 15pF$ , $R_L = 390\Omega$		25	50	ns	
$t_{TLH}$ Transition time, low-to-high-level output		$C_L = 15pF$ , $R_L = 3.9k\Omega$			120	175	ns
$t_{THL}$ Transition time, high-to-low-level output		$C_L = 15pF$ , $R_L = 390\Omega$			10	20	ns

## PARAMETER MEASUREMENT INFORMATION§



$I_{CC}$  is tested for all four receivers simultaneously



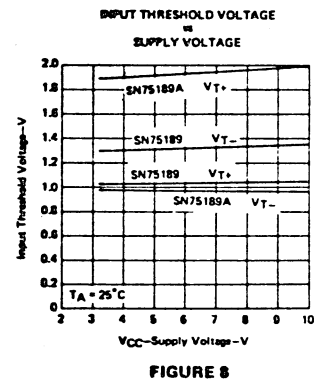
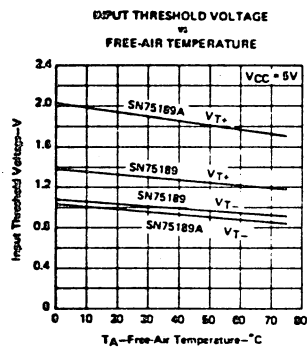
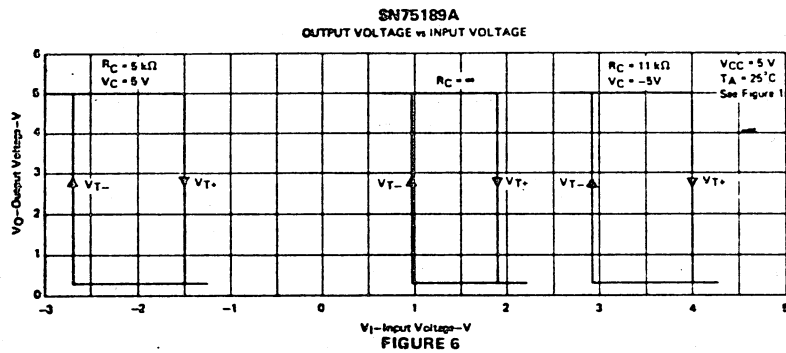
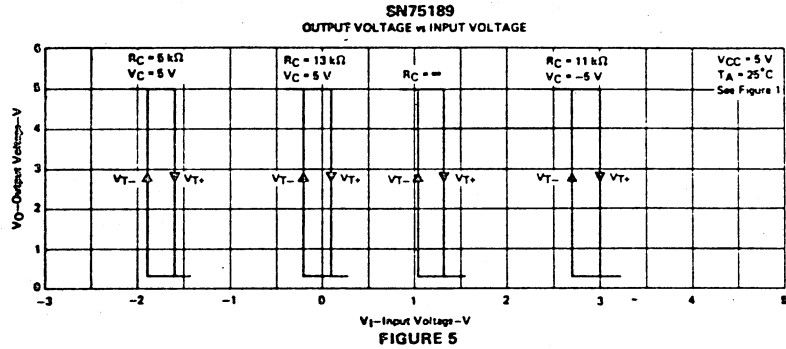
- NOTES: A. The pulse generator has the following characteristics:  $Z_{out} \approx 50\Omega$ ,  $t_w = 500ns$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3564 or equivalent.

FIGURE 4—SWITCHING TIMES

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

# TYPES SN75189, SN75189A QUADRUPLE LINE RECEIVERS

## TYPICAL CHARACTERISTICS



## Subsection 7.2.5

### Current Loop Transistors

This subsection includes specifications for the 2N223/3A transistors used in the input/output circuits of the optoisolated current loops. Note there are two separate transistors in each can. The two collectors are on either side of the tab. Continuing away from the tab, the two bases are next with the two emitters adjacent to each other and across from the tab. The device has multiple sources so units from vendors other than Texas Instruments may be found on the DK611-A.

# TYPES 2N2060, 2N2223, 2N2223A DUAL N-P-N SILICON TRANSISTORS

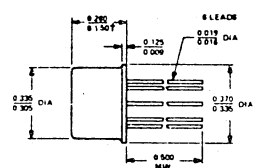
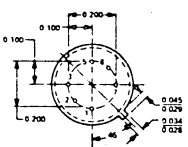
BULLETIN NO. DL-S 7211678, MARCH 1972

## TWO TRANSISTORS IN ONE PACKAGE FOR DIFFERENTIAL AMPLIFIER APPLICATIONS

- Medium Power
- High Operating Voltage

### \*mechanical data


ALL LEADS INSULATED FROM CASE

ALL DIMENSIONS ARE IN INCHES  
UNLESS OTHERWISE SPECIFIED

Dimensions without tolerance designate true position. Leads having maximum diameter (0.019") measured in gaging plane 0.054" +0.001" -0.000" below the seating plane of the device shall be within 0.007" of their true position relative to a maximum width tab.

1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
5. EMITTER 2
6. BASE 2
7. COLLECTOR 2



† Applicable to 2N2223 and 2N2223A only. Registered minimum dimension for 2N2060 is 0.140.

### \*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	2N2060		2N2223 2N2223A		UNIT
	EACH TRIODE	TOTAL DEVICE	EACH TRIODE	TOTAL DEVICE	
Collector-Base Voltage	100		100		V
Collector-Emitter Voltage (See Note 1)	80		80		V
Collector-Emitter Voltage (See Note 2)	60		60		V
Emitter-Base Voltage	7		7		V
Continuous Collector Current	500		500		mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	0.5	0.6	0.5	0.6	W
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Notes 4 and 5)	1.5	3	1.6	3	W
Continuous Device Dissipation at 100°C Case Temperature	0.86	1.7	0.91	1.7	W
Operating Collector Junction Temperature	200		200		°C
Storage Temperature Range	-65°C to 200°C				
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C				

- NOTES:
1. These values apply when the base-emitter resistance ( $R_{BE}$ ) is equal to or less than 10 ohms.
  2. These values apply when the base-emitter diode is open-circuited.
  3. Derate linearly to 200°C free-air temperature at the rate of 2.86 mW/°C for each triode and 3.43 mW/°C for total device.
  4. Derate 2N2060 linearly to 200°C case temperature at the rate of 8.6 mW/°C for each triode and 17.2 mW/°C for total device.
  5. Derate 2N2223 and 2N2223A linearly to 200°C case temperature at the rate of 9.1 mW/°C for each triode and 17.2 mW/°C for total device.
  6. The terminals of the triode not under test are open-circuited for the measurement of these characteristics.
  7. This parameter must be measured using pulse techniques.  $t_w = 300 \mu s$ , duty cycle  $\leq 1\%$ .
  8. The lower of the two  $h_{FE}$  reading is taken as  $h_{FE1}$ .
  9. This parameter is measured in an amplifier with response down 3 dB at 25 Hz and 10 kHz and a high-frequency rolloff of 6 dB/octave.

\*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

USES CHIP N23

**TEXAS INSTRUMENTS**  
INCORPORATED  
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

# TYPES 2N2060, 2N2223, 2N2223A DUAL N-P-N SILICON TRANSISTORS

\*electrical characteristics at 25°C free-air temperature (unless otherwise noted)  
individual triode characteristics (see note 6)

PARAMETER	TEST CONDITIONS	2N2060		2N2223 2N2223A		UNIT	
		MIN	MAX	MIN	MAX		
V(BR)CBO	Collector-Base Breakdown Voltage $I_C = 100 \mu A, I_E = 0$	100		100		V	
V(BR)CEO	Collector-Emitter Breakdown Voltage $I_C = 30 \text{ mA}, I_B = 0$ , See Note 7	60		60		V	
V(BR)CER	Collector-Emitter Breakdown Voltage $I_C = 100 \text{ mA}, R_{BE} = 10 \Omega$ , See Note 7	80		80		V	
V(BR)EBO	Emitter-Base Breakdown Voltage $I_E = 100 \mu A, I_C = 0$	7		7		V	
I <sub>CBO</sub>	Collector Cutoff Current $V_{CB} = 80 \text{ V}, I_E = 0$		2		10	nA	
I <sub>EBO</sub>	Emitter Cutoff Current $V_{EB} = 5 \text{ V}, I_C = 0$		2		10	nA	
h <sub>FE</sub>	Static Forward Current Transfer Ratio $V_{CE} = 5 \text{ V}, I_C = 10 \mu A$		25	75	15		
			30	90	25	150	
			40	120			
			50	150	50	200	
V <sub>BE</sub>	Base-Emitter Voltage $I_B = 5 \text{ mA}, I_C = 50 \text{ mA}$		0.9		0.9	V	
V <sub>CE(sat)</sub>	Collector-Emitter Saturation Voltage $I_B = 5 \text{ mA}, I_C = 50 \text{ mA}$		1.2		1.2	V	
h <sub>ib</sub>	Small-Signal Common-Base Input Impedance $V_{CB} = 5 \text{ V}, I_C = 1 \text{ mA}, f = 1 \text{ kHz}$	20	30	20	30	$\Omega$	
h <sub>rb</sub>	Small-Signal Common-Base Reverse Voltage Transfer Ratio				$3 \times 10^{-4}$		
h <sub>ob</sub>	Small-Signal Common-Base Output Admittance				0.5	$\mu\text{mho}$	
h <sub>ie</sub>	Small-Signal Common-Emitter Input Impedance $V_{CE} = 5 \text{ V}, I_C = 1 \text{ mA}, f = 1 \text{ kHz}$	1000	4000			$\Omega$	
h <sub>fe</sub>	Small-Signal Common-Emitter Forward Current Transfer Ratio	50	150	40	200		
h <sub>oe</sub>	Small-Signal Common-Emitter Output Admittance		16			$\mu\text{mho}$	
h <sub>fe</sub>	Small-Signal Common-Emitter Forward Current Transfer Ratio $V_{CE} = 10 \text{ V}, I_C = 50 \text{ mA}, f = 20 \text{ MHz}$		3		2.5		
C <sub>obo</sub>	Common-Base Open-Circuit Output Capacitance $V_{CB} = 10 \text{ V}, I_E = 0, f = 1 \text{ MHz}$		15		15	pF	
C <sub>ibo</sub>	Common-Base Open-Circuit Input Capacitance $V_{EB} = 0.5 \text{ V}, I_C = 0, f = 1 \text{ MHz}$		85		85	pF	

### triode matching characteristics

PARAMETER	TEST CONDITIONS	2N2060		2N2223		2N2223A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
h <sub>FE1</sub>	Static Forward Current $V_{CE} = 5 \text{ V}, I_C = 100 \mu A$ , See Note 8	0.9	1	0.8	1	0.9	1	
h <sub>FE2</sub>	Gain Balance Ratio $V_{CE} = 5 \text{ V}, I_C = 1 \text{ mA}$ , See Note 8	0.9	1					
V <sub>BE1</sub> - V <sub>BE2</sub>	Base-Emitter-Voltage Differential $V_{CE} = 5 \text{ V}, I_C = 100 \mu A$		5		15		5	mV
					5			
$\frac{\Delta(V_{BE1} - V_{BE2})}{\Delta T_A}$	Base-Emitter-Voltage-Differential Temperature Gradient $V_{CE} = 5 \text{ V}, I_C = 100 \mu A$ , From $T_A = -55^\circ\text{C}$ to $T_A = 125^\circ\text{C}$		10		25		25	$\mu\text{V}/^\circ\text{C}$

\*operating characteristics at 25°C free-air temperature  
individual triode characteristics (see note 6)

PARAMETER	TEST CONDITIONS	2N2060		UNIT
		MIN	MAX	
F	Spot Noise Figure $V_{CE} = 10 \text{ V}, I_C = 300 \mu A, R_G = 510 \Omega, f = 1 \text{ kHz}$		8	dB
F	Average Noise Figure $V_{CE} = 10 \text{ V}, I_C = 300 \mu A, R_G = 1 \text{ k}\Omega$ , Noise Bandwidth = 15.7 kHz, See Note 9		8	dB

\*JEDEC registered data

### Subsection 7.2.6

#### Optoisolator, 4N35

Four 4N35 optical isolators are used in the current loop circuits to provide isolation between the logic and the current loops. The specifications included are for General Electric's version but the circuit may be supplied by other vendors. Note that the specifications are generally stated at an optimum point ( $25^{\circ}\text{C}$ ,  $I_f = 10\text{ma}$  and  $V_{CE} = 10$  volts) and deviations from these can cause significant changes in the specifications.

# OPTOELECTRONICS



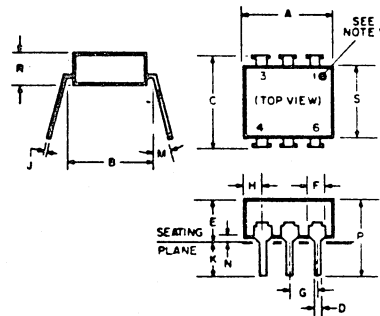
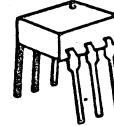
## Photon Coupled Isolator 4N35-4N36-4N37

Ga As Infrared Emitting Diode & NPN Silicon Photo-Transistor

The General Electric 4N35-4N36-4N37 are gallium arsenide infrared emitting diodes coupled with a silicon photo-transistor in a dual in-line package.

**FEATURES:**

- Fast switching speeds
- High DC current transfer ratio
- High isolation resistance
- High isolation voltage
- I/O compatible with integrated circuits
- Covered under U.L. component recognition program, reference file E51868



absolute maximum ratings: (25°C) (unless otherwise specified)

INFRARED EMITTING DIODE			
• Power Dissipation	$T_A = 25^\circ\text{C}$	☆100	milliwatts
• Power Dissipation	$T_C = 25^\circ\text{C}$	☆100	milliwatts
(T <sub>C</sub> indicates collector lead temperature 1/32" from case)			
• Forward Current (Continuous)		60	milliamps
• Forward Current (Peak)		3	ampere
(Pulse width 1 usec, 300 pps)			
• Reverse Voltage		6	volts

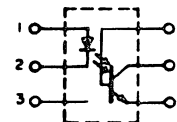
☆Derate 1.33mW/°C above 25°C

PHOTO-TRANSISTOR			
• Power Dissipation	$T_A = 25^\circ\text{C}$	☆☆300	milliwatts
• Power Dissipation	$T_C = 25^\circ\text{C}$	☆☆500	milliwatts
(T <sub>C</sub> indicates collector lead temperature 1/32" from case)			
• V <sub>CEO</sub>		30	volts
• V <sub>CBO</sub>		70	volts
• V <sub>ECO</sub>		7	volts
• Collector Current (Continuous)		100	milliamps

☆☆Derate 4.0mW/°C above 25°C  
☆☆☆Derate 6.7mW/°C above 25°C

SYMBOL	INCH		MILLIMETER		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.330	REF	3.08	3.8	REF
B	.300	REF	7.62	REF	2
C			.340		8.64
D	.016	.020	4.06	5.08	3
E			.200		5.08
F	.040	.070	.01	1.78	4
G	.090	1.10	2.28	2.79	
H		.085		2.16	5
J	.008	.012	2.03	3.05	
K	.100		2.54		3
M		15°		15°	
N	.015		3.81		3
P		.375		9.53	
R	.100	1.85	2.54	47.0	
S	.225	2.80	5.71	7.12	

- NOTES
1. There shall be a permanent indication of terminal orientation in the quadrant adjacent to terminal 1.
  2. Installed position lead centers.
  3. Overall installed dimension.
  4. These measurements are made from the seating plane.
  5. Four places.



TOTAL DEVICE			
• Storage Temperature	-55 to 150°C		
• Operating Temperature	-55 to 100°C		
• Lead Soldering Time (at 260°C)	10 seconds.		
• Relative Humidity	85% @ 85°C		
• Input to Output Isolation Voltage			
4N35	2500 V <sub>(RMS)</sub>	3550 V <sub>(peak)</sub>	
4N36	1750 V <sub>(RMS)</sub>	2500 V <sub>(peak)</sub>	
4N37	1050 V <sub>(RMS)</sub>	1500 V <sub>(peak)</sub>	

individual electrical characteristics (25°C) (unless otherwise specified)

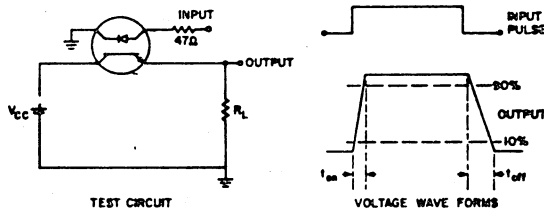
INFRARED EMITTING DIODE	SYMBOL	MIN.	MAX.	UNITS	PHOTO-TRANSISTOR	SYMBOL	MIN.	TYP.	MAX.	UNITS
* Forward Voltage (I <sub>F</sub> = 10 mA)	V <sub>F</sub>	.8	1.5	volts	* Breakdown Voltage (I <sub>C</sub> = 10 mA, I <sub>F</sub> = 0)	V(BR) CEO	30	-	-	volts
* Forward Voltage (I <sub>F</sub> = 10 mA) T <sub>A</sub> = -55°C	V <sub>F</sub>	.9	1.7	volts	* Breakdown Voltage (I <sub>C</sub> = 100uA, I <sub>F</sub> = 0)	V(BR) CBO	70	-	-	volts
* Forward Voltage (I <sub>F</sub> = 10 mA) T <sub>A</sub> = +100°C	V <sub>F</sub>	.7	1.4	volts	* Breakdown Voltage (I <sub>F</sub> = 100uA, I <sub>F</sub> = 0)	V(BR) ECO	7	-	-	volts
* Reverse Current (V <sub>R</sub> = 6V)	I <sub>R</sub>	-	10	microamps	Collector Dark Current (V <sub>CE</sub> = 10V, I <sub>F</sub> = 0)	I <sub>CEO</sub>	-	5	50	nanoamps
Capacitance (V=0, f=1 MHz)	C <sub>J</sub>	-	100	picofarads	* Collector Dark Current (V <sub>CE</sub> = 30V, I <sub>F</sub> = 0) T <sub>A</sub> = 100°C	I <sub>CEO</sub>	-	-	500	microamps
					Capacitance (V <sub>CE</sub> = 10V, f = 1MHz)	C <sub>CE</sub>	-	2	-	picofarads

coupled electrical characteristics (25°C) (unless otherwise specified)

	MIN.	TYP.	MAX.	UNITS
* DC Current Transfer Ratio (I <sub>F</sub> = 10mA, V <sub>CE</sub> = 10V)	100	-	-	%
* DC Current Transfer Ratio (I <sub>F</sub> = 10mA, V <sub>CE</sub> = 10V) T <sub>A</sub> = -55°C	40	-	-	%
* DC Current Transfer Ratio (I <sub>F</sub> = 10mA, V <sub>CE</sub> = 10V) T <sub>A</sub> = +100°C	40	-	-	%
* Saturation Voltage—Collector To Emitter (I <sub>F</sub> = 10mA, I <sub>C</sub> = 0.5mA)	-	-	0.3	volts
* Input to Output Isolation Current (Pulse Width = 8 msec)				
(See Note 1) Input to Output Voltage = 3550 V <sub>(peak)</sub> 4N35	-	-	100	microamps
Input to Output Voltage = 2500 V <sub>(peak)</sub> 4N36	-	-	100	microamps
Input to Output Voltage = 1500 V <sub>(peak)</sub> 4N37	-	-	100	microamps
* Input to Output Resistance (Input to Output Voltage = 500V - See Note 1)	100	-	-	gigaohms
* Input to Output Capacitance (Input to Output Voltage = 0, f = 1MHz - See Note 1)	-	-	2.5	picofarads
* Turn on Time - t <sub>on</sub> (V <sub>CC</sub> = 10V, I <sub>C</sub> = 2MA, R <sub>L</sub> = 100Ω) (See Figure 1)	-	5	10	microseconds
* Turn off Time - t <sub>off</sub> (V <sub>CC</sub> = 10V, I <sub>C</sub> = 2MA, R <sub>L</sub> = 100Ω) (See Figure 1)	-	5	10	microseconds

Note 1: Tests of input to output isolation current resistance, and capacitance are performed with the input terminals (diode) shorted together and the output terminals (transistor) shorted together

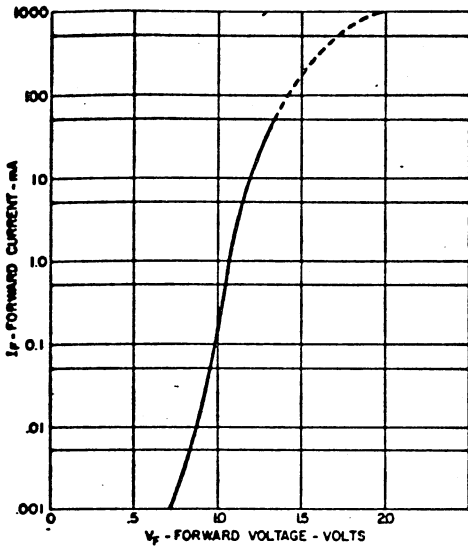
\* Indicates JEDEC registered values.



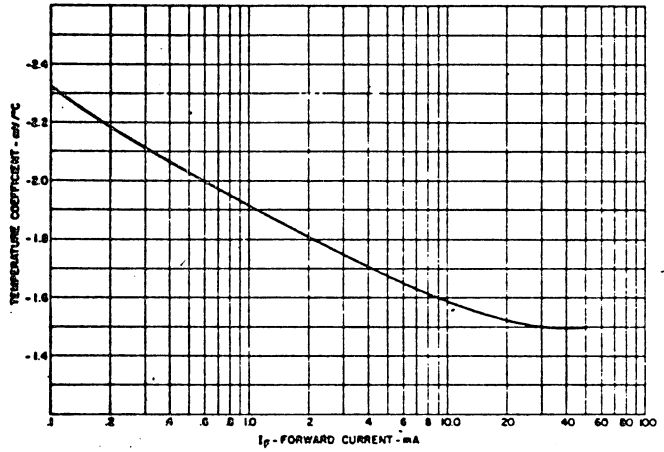
Adjust Amplitude of Input Pulse for Output (I<sub>C</sub>) of 2 mA

FIGURE 1

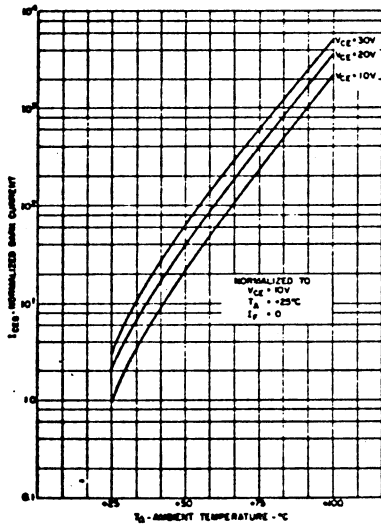
# TYPICAL CHARACTERISTICS



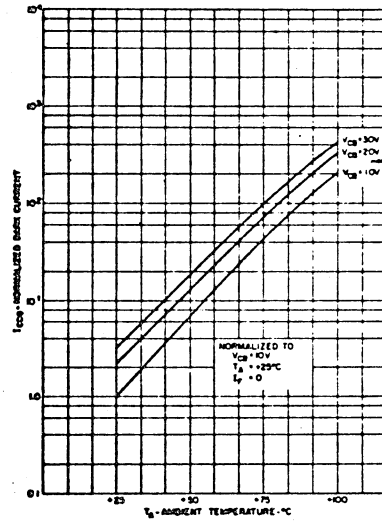
1. INPUT CHARACTERISTICS



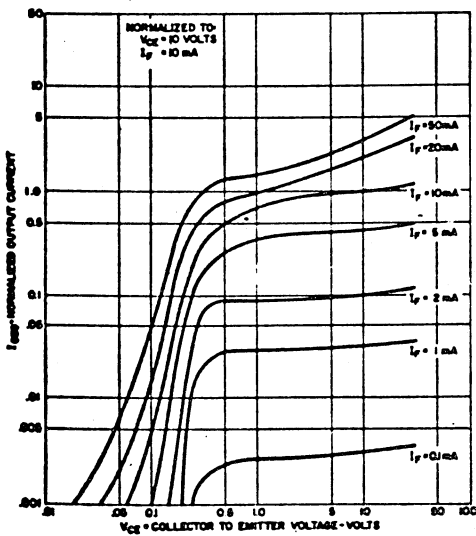
2. FORWARD CURRENT TEMPERATURE COEFFICIENT



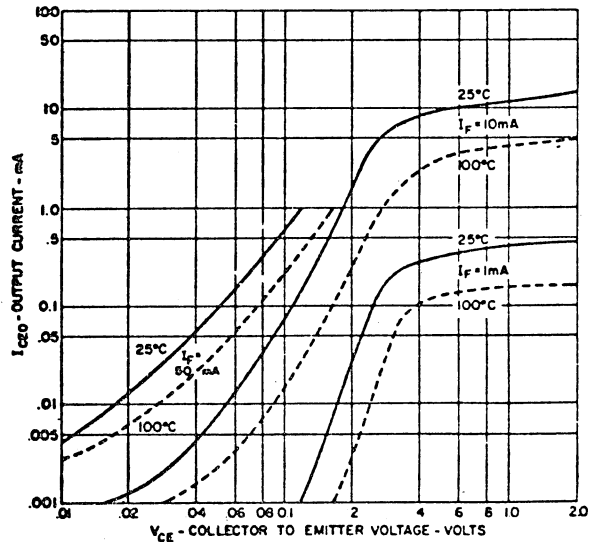
3. DARK  $I_{CEO}$  CURRENT VS TEMPERATURE



4.  $I_{CBO}$  VS TEMPERATURE



5. OUTPUT CHARACTERISTICS



6. OUTPUT CHARACTERISTICS

## APPENDIX A

### JUMPER MODULE OPTIONS

#### A.1 Signal Groups

Mode of communication (RS232 or current-mode), Clear-to-Send Enable to control transmit data and determination of a Mark (current flow or not) are functions that are selectable by the jumper module at E8. The jumper module is necessary because RS232 and current-mode data outputs and inputs share common connector pins on the external connector. Figure A.1 is the basic jumper module with the input/output signals and the intra-pin clad jumpers shown. It should be noted that with the exception of pins 13-16 all the jumpers are concerned with either transmit or receive data.

##### A.1.1 Marking Sense Control

Pins 13 and 16 on the module are used to control the sense of a Mark in current loop operation. If the connection is left open (as it is shipped standard), a Mark indicates current flowing in the loop. This is the standard Teletype<sup>®</sup> convention and a space or no current flow causes a line break to be detected. Connecting pin 13 to 16 on the module inverts the sense for the Transmit, Receive and Restraint circuits such that a Mark equals no current flow. This option is included because some peripherals use this logic sense to reduce power consumption in the quiescent (Mark) condition.

<sup>®</sup> Registered trademark of Teletype Corp.

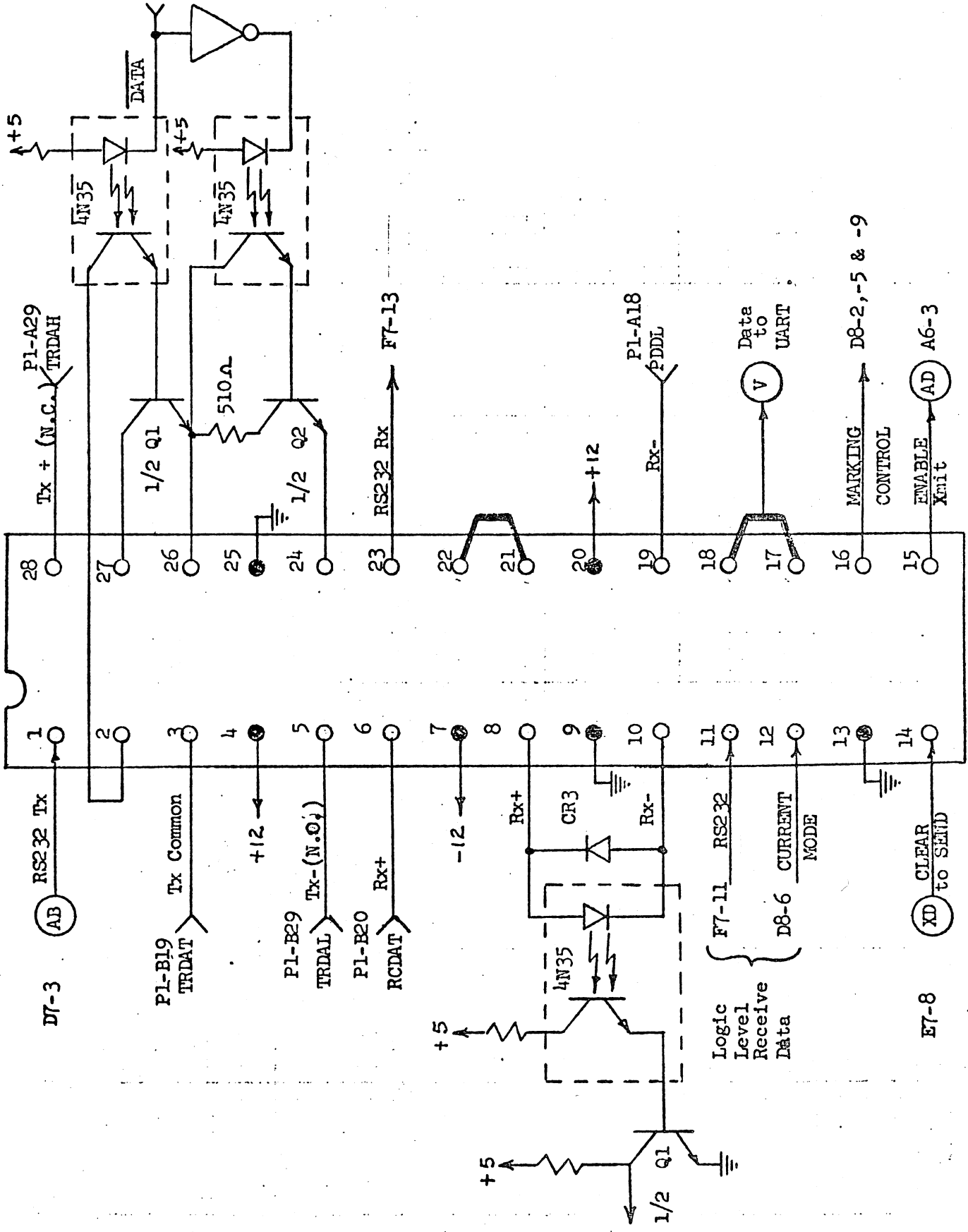


Figure A.1 Serial I/O Jumper Module

### A.1.2 CTS Restraint Enable

Pins 14 and 15 are part of the Clear to Send (CTS) restraint circuit which can be used in RS232 operation, only, to inhibit (restrain) the transmission of data to an external peripheral. A peripheral or modem can inhibit transmission of data by dropping its Clear to Send signal. For example, a printer terminal might drop CTS if its buffer was nearly full. Although labeled as inhibit transmit, the signal actually inhibits the UART from requesting data from the CPU. It is possible that if the UART transmit section is full, up to two more characters could be transmitted after the CTS signal is dropped. This CTS enable signal can be used even if the external device does not have a Clear to Send signal. For example an external power on signal can be input which would inhibit data transmission if the remote device is off. The CTS signal input should be greater than +3v in the "on" condition.

### A.1.3 Transmit Output Data

Pin 3 is connected to B19 (TRDAT) of the output connector. A jumper from pin 1 to 3 will connect the RS232 transmit data from D7-3 to the output connector. Current operation requires two outputs for a continuous loop. For unipolar operation the positive terminal of the loop supply is connected to pin 28 (or A29 if supplied externally) which is connected via pins 2 and 27 to the collector of Q1. Pin 26, the emitter of Q1, is connected to output pin B19 via a jumper between pins 3 and 26. For bipolar operation, a negative loop supply is connected to pin 5 (or B29 if supplied externally) which is connected to the emitter of Q2 via pin 24. Current-limiting resistors may be

found between the pins 2 and 27 and/or 5 and 24. Note there is a fixed 510 ohm current-limiting resistor in the collector circuit of Q2.

#### A.1.4 Input Receive Data

Receive data (RCDAT) from B20 of the connector is brought into pin 6 of the jumper module. By jumpering pin 6 to 23, RCDAT is connected to an input (pin 13) of the quad RS232 receiver, F7. If pin 6 is jumpered to 22 and 21 connected to pin 8 (21 and 22 are connected on the board), RCDAT is connected to the anode of the photo-diode receive circuit, C8B-1. Normally, a current-limiting resistor is connected from pin 21 to 8 of the module. The cathode of the photo-diode receive circuit, C8B-2, is connected to pin 10 of the jumper module which if jumpered to pin 19 connects the other loop input, photo-diode low (PDDL), A18 to the circuit.

#### A.1.5 Logic Level Receive Data

Another set of jumpers connects either the RS232 or current-loop receive data to the serial data input of the UART. Pins 17 and 18 of the jumper module are connected to the UART receive data input, DE2-20. If pin 11 is jumpered to pin 18, RS232 data is connected to the UART. If instead, pin 12 is jumpered to 17, current-loop data is input to the UART.

Communication System Types

The SIO is designed to interface RS-232-C compatible and nominal 20 to 40 ma current loop devices. The EIA RS-232-C specification uniquely defines the interface signals; however, current loop operation is defined only to the extent that a current loop must have a send circuit, a receive circuit and a loop power supply which are all in series or in a loop. In full duplex operation, the SIO transmitter would be connected via a current loop to the receive circuit of a remote device. On a separate loop the SIO receiver would be connected to a remote transmitter. There are a number of variations of current loop systems which differ primarily in the supply of loop power. The following describes a typical RS-232 configuration and then follows with a number of current loop systems which are, in turn, related to specific jumper modules. Jumpers on the jumper module are shown as dashed lines and the numbers above the circle refer to pins on the module. When viewing the module from the top the cutout or index is closest to pin 1 and the pins run counter clockwise with pin 28 opposite pin 1.

A.2.1 RS-232-C

For interfacing RS232-compatible devices the RS232 transmitter and receiver are connected to the external connector pins B19 and B20, respectively. The TTL logic-level data is connected to the UART receive data input and the Clear-to-Send signal, if used, can inhibit transmit data. These connections are shown in a simplistic logic diagram as follows

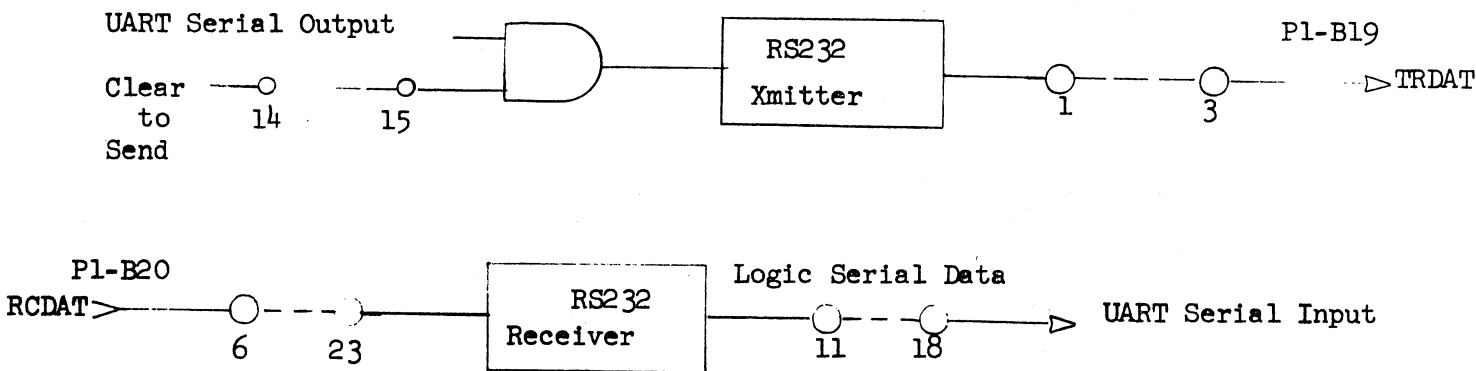
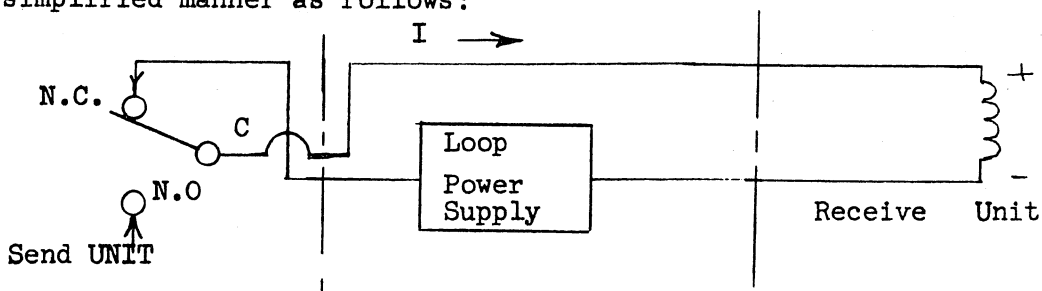


Figure A.2 RS232 Connections

A.2.2 Current Loop

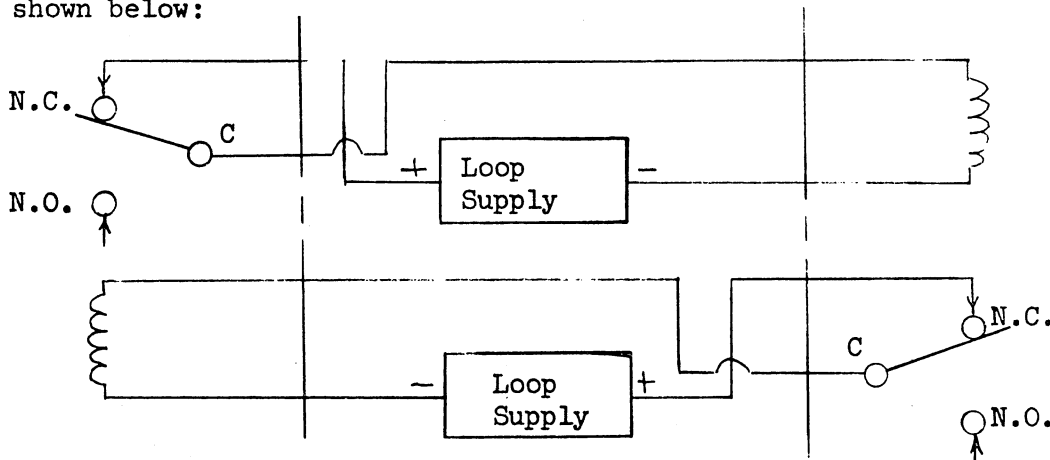
Current Loop devices are used to provide data communications in the presence of high common mode voltages. In a properly designed current loop circuit, the loop is isolated from the computer on one end and a remote device on the other.

A current loop consists of a sending unit (transmitter), a receiving unit and a loop power supply in a series type circuit. This can be shown in a simplified manner as follows:



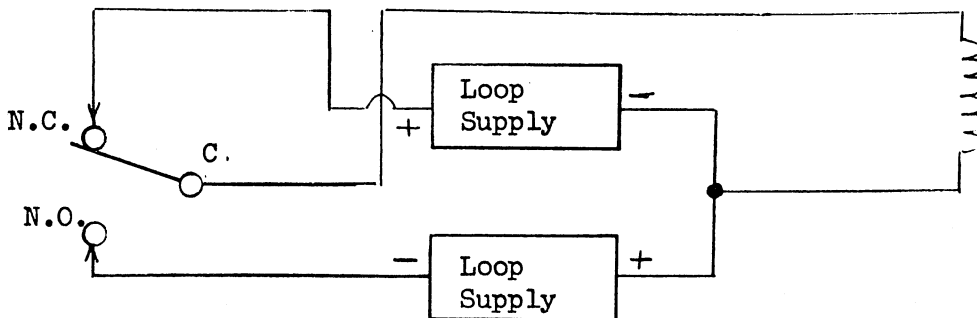
In this circuit current flows as long as the normally closed (N.C.) contacts make. When the common (C) is connected to the normally open (N.O.) contacts the loop is open and no current flows. This type of current loop is defined as unipolar and the two logic states of the circuit are current flow or an open circuit (line break) with no current flow.

For a full duplex operation two separate loops would be used as shown below:



This is probably the most general case - two separate unipolar loops.

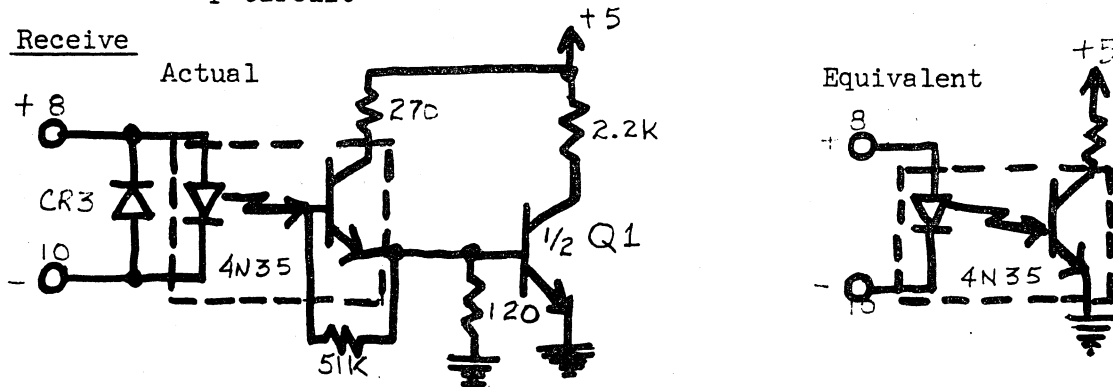
A bipolar current loop is defined as a current loop with two loop supplies. The two supplies have opposite polarities with one connected to the n.c. contacts and the other to the n.o. contacts as shown below:



In this type of loop, there are three logic states - 1) current flow in one direction, 2) current flow in the opposite direction and 3) an open circuit (line break) with no current flow. Bipolar operation is particularly useful for long lines as current is pumped in both directions which minimizes the effect of long cable runs.

Although the diagrams shown above have shown the loop supply as being separate from the send or receive units, in most cases one or the other supplies the loop voltage.

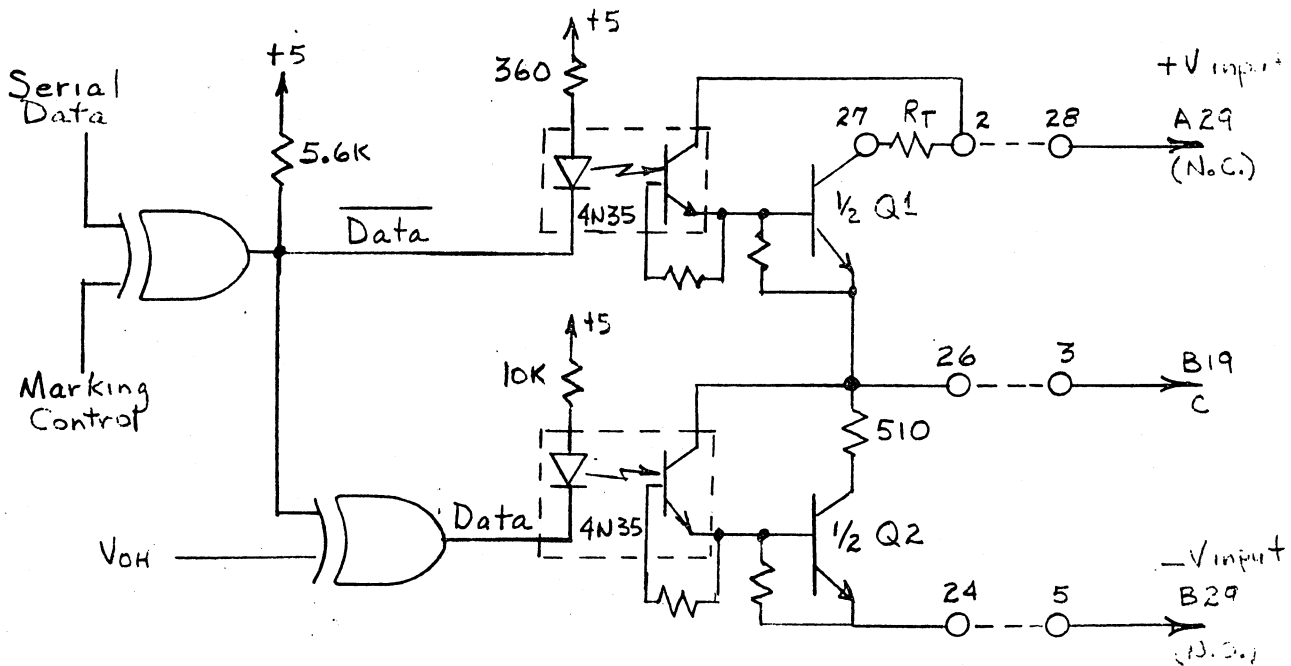
### A.2.2.1 Current Loop Circuit



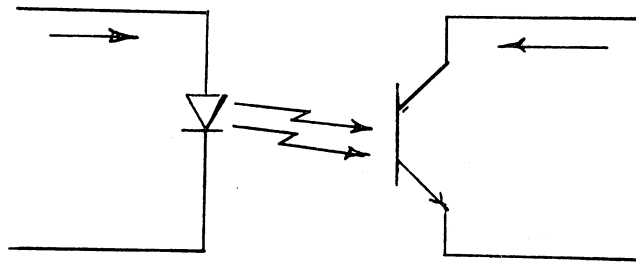
CR3 is used to prevent reverse voltage from breaking down the LED. The output of the 4N35 and Q1 form a non-inverting amplifier so the output can be approximated by the 4N35 output only.

### Transmit

The actual SIO transmit circuit looks like the following:



As in the receive circuit, if the output of the 4N35 and its output transistor are combined the following simplified circuit results:



The simplified circuits will be used in the next section to define a number of current loop types.

#### A.2.2.2 Externally-Powered Loops

Connections to the SIO are the same regardless whether a separate loop supply is used or the remote device powers the loop. For a unipolar loop a loop supply voltage must be input with the SIO completing the loop to the remote device. The basic configuration is two separate loops each of which has a loop supply. A variation is to use one supply for both loops and merging the loops by having a common power lead. This variation reduces the cabling costs since only three signals are needed for full duplex as opposed to four for separate loops.

### Separate Send and Receive Loops

Figure A.3 below illustrates two independent send and receive loops. Although the Figure shows the loop supplies as being external to both the SIO and the remote terminal, the same SIO connections would be needed even if the remote terminal contained the loop supply. Note that  $R_T$  and  $R_R$  are current-limiting resistors for the SIO transmit and receive loops, respectively.

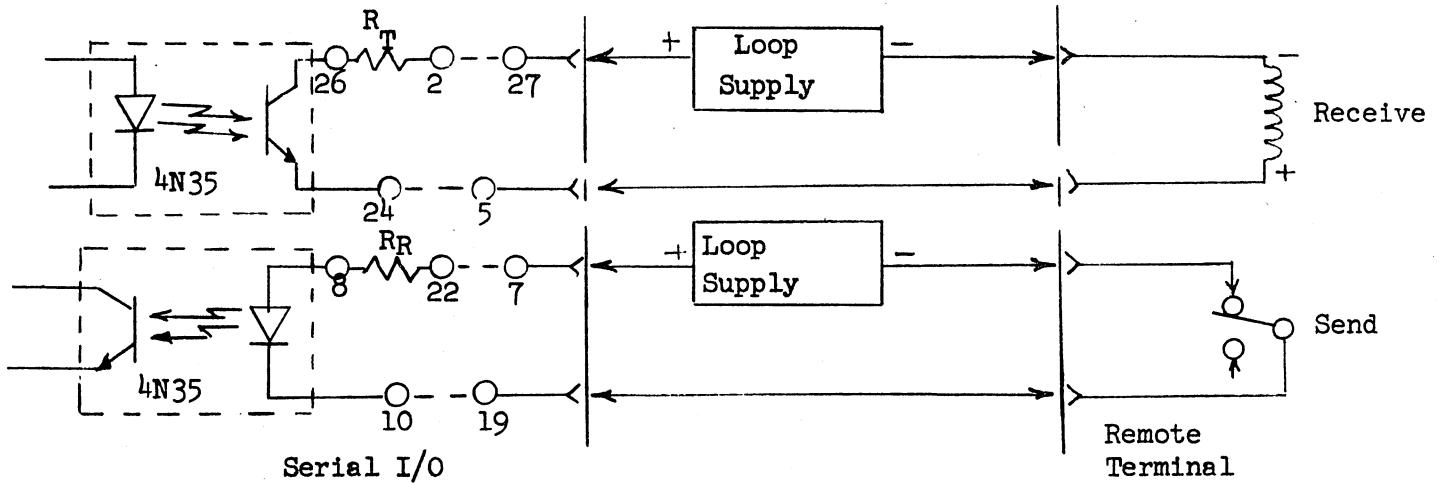


Figure A.3 - Separate Send and Receive Loops

### Common Lead Loops

A number of terminals use a system whereby a single loop supplies powers both loops of a full duplex system. In this system only three leads (power, loop 1 and loop 2) are needed at either the SIO or the remote terminal. Since the terminal is the device which determines this mode, all references to the common power lead will be referenced to the terminal side of the loop. Configurations of the SIO in a common positive and negative loops are shown in the next two figures.

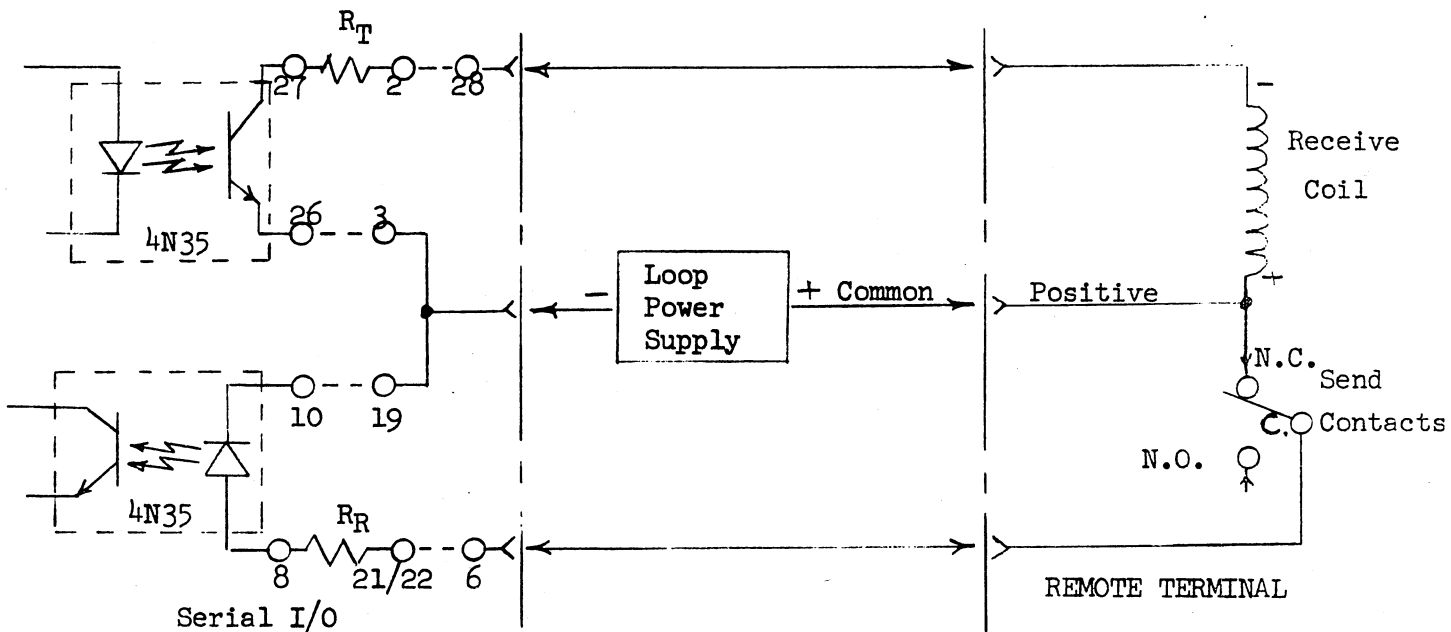


FIGURE A.4 - COMMON POSITIVE LOOPS

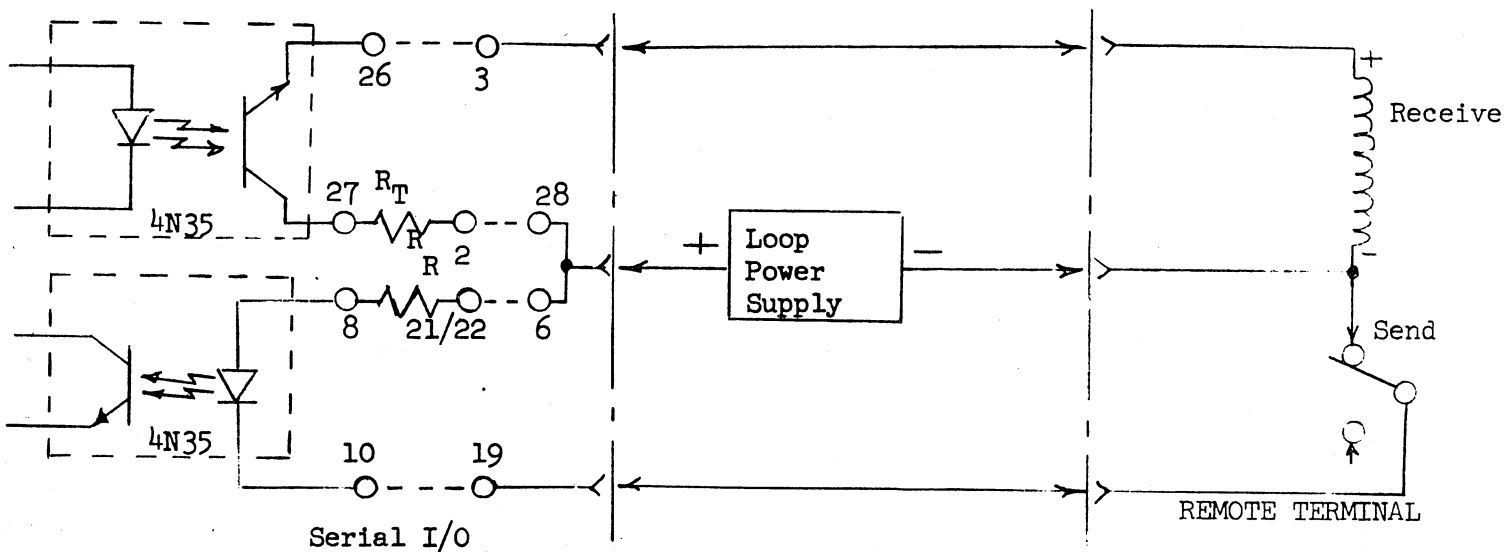


FIGURE A.5 - COMMON NEGATIVE LOOPS

A.2.2.3 SIO Powered Loops

The SIO can provide +12 volts and ground for unipolar loops or  $\pm 12$  volts for bipolar loops. In these configurations, there is a reduction in isolation since the computer ground becomes part of the current loop circuit. As shown above, there is the general case of two distinct loops; however, note that the same supply (+12V for unipolar) powers both loops. The common positive or negative configurations are nearly the same as the externally-powered versions.

Figure A.6, below, illustrates SIO configurations for separate loops.

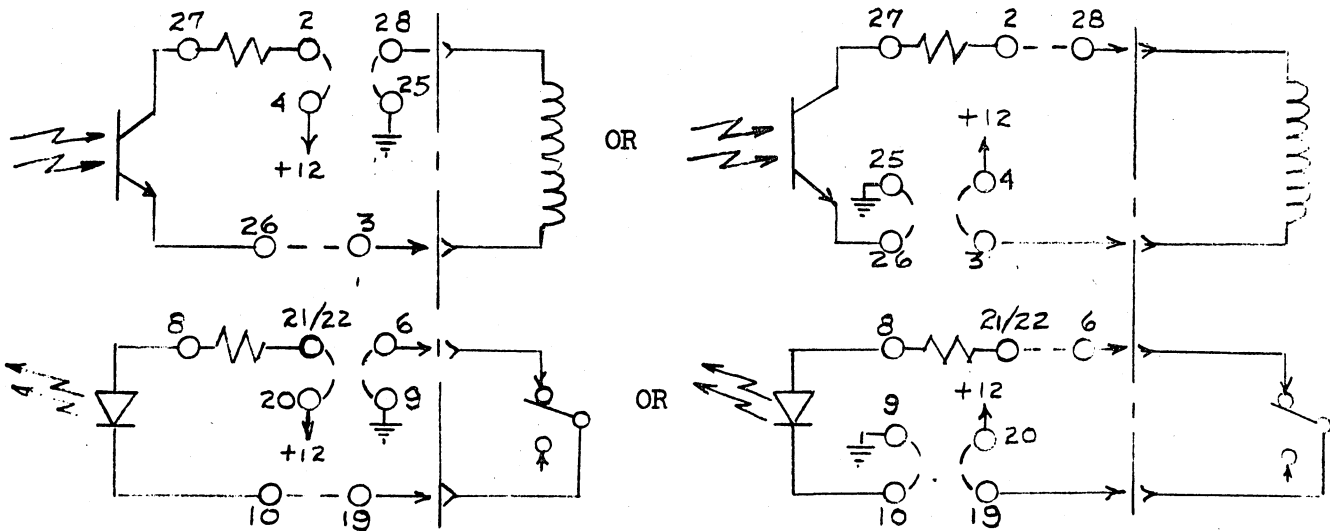


Figure A.6 Separate Loops, SIO Provides Power

The next two figures illustrate common positive and negative loops when the SIO supplies the +12 volts in a unipolar configuration.

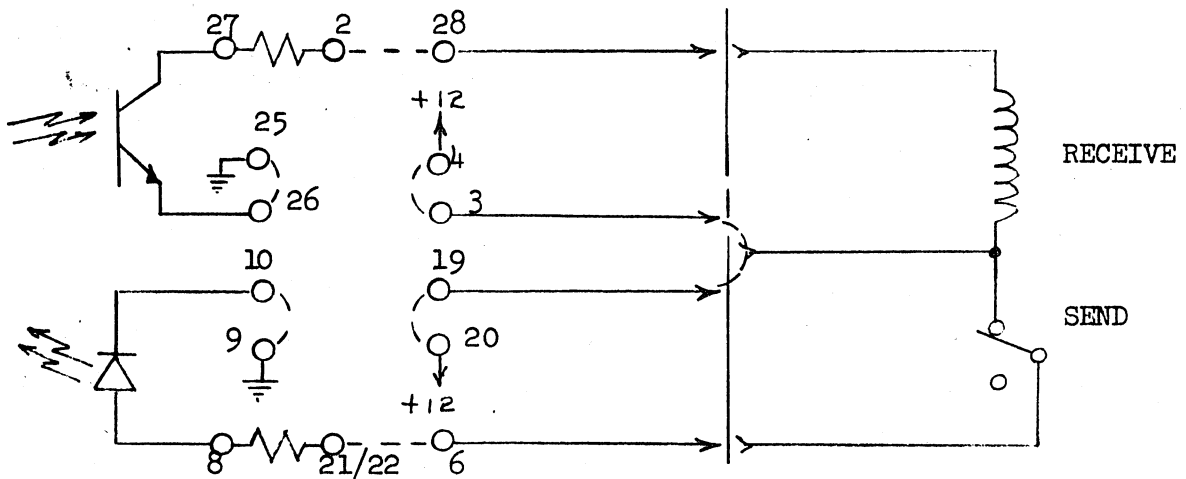


Figure A.7 SIO Supplies Common Positive Loops

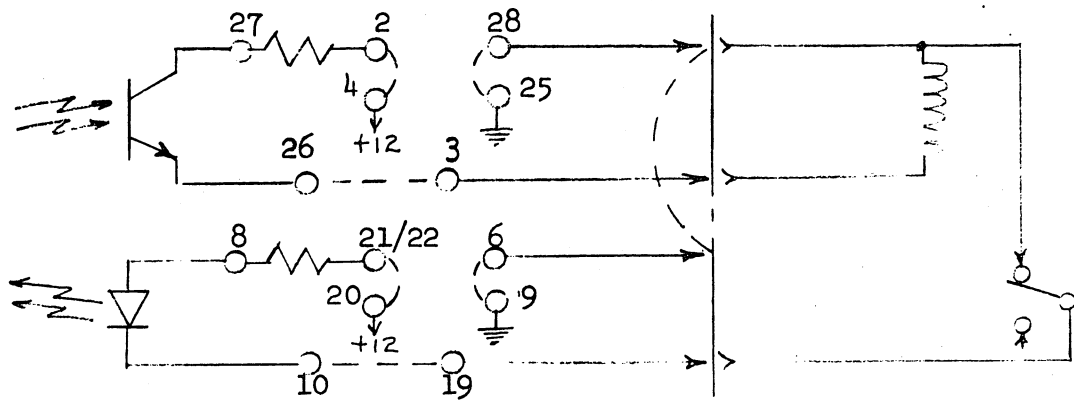


Figure A.8 SIO Supplies Common Negative Loops

There are mixed versions of the separate loops whereby the SIO provides power for one loop and the other loop is supplied externally but these are only variations of the above.

### Bipolar Operations

Referring to Figure A.1 it can be seen that only the transmit section of the SIO needs to be configured for bipolar current loops. In this mode the common lead of the power supply would be connected to the cathode of the photodiode (pin 10) of the receive circuit while the received data line would connect from pin 7 to 21/22 through a limiting resistor (if necessary) to pin 8. CR3 will shunt the negative going voltage to avoid damage to the photo-diode. For bipolar transmission, the negative voltage would be applied to pin 5 (connector pin B29) externally or from pin 7 (-12v) internally. A current-limiting resistor might be needed between pins 5 and 24; however, there already is a 510 Ohm resistor in the collector circuit of Q2 so additional resistance may not be needed.

Current Loop Circuit Jumpers and Restrictions

In order to provide the number of variations described above, the SIO transmit and receive circuits have to have the capability via the jumper module of accepting external loop voltages or providing +12 volts and ground (or +12 volts for bipolar) for loops that the SIO powers. The following two figures show potential connections for the transmit and receive circuits.

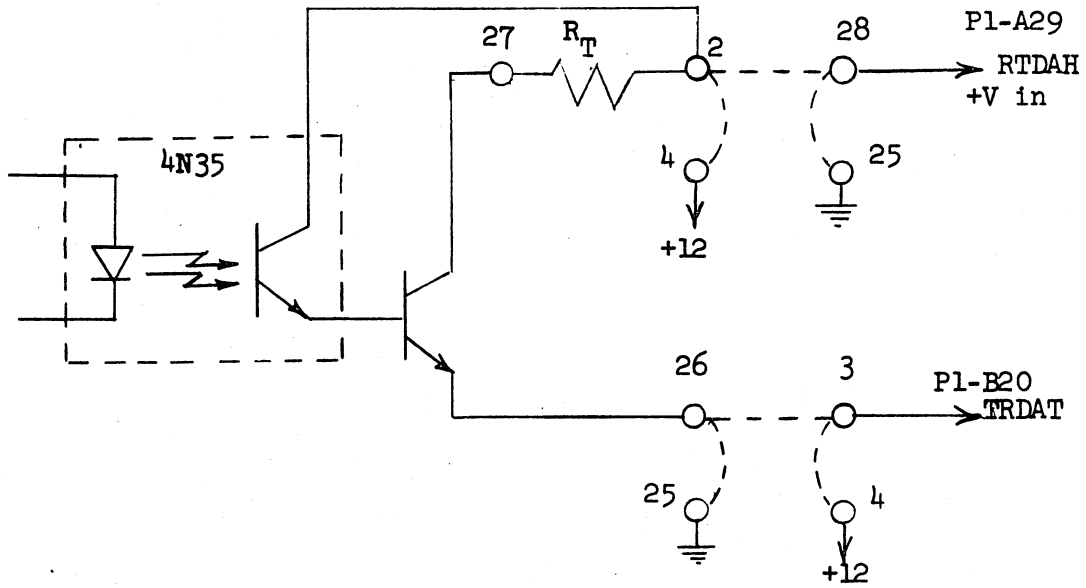


Figure A.9 Current Loop Transmit Jumpers

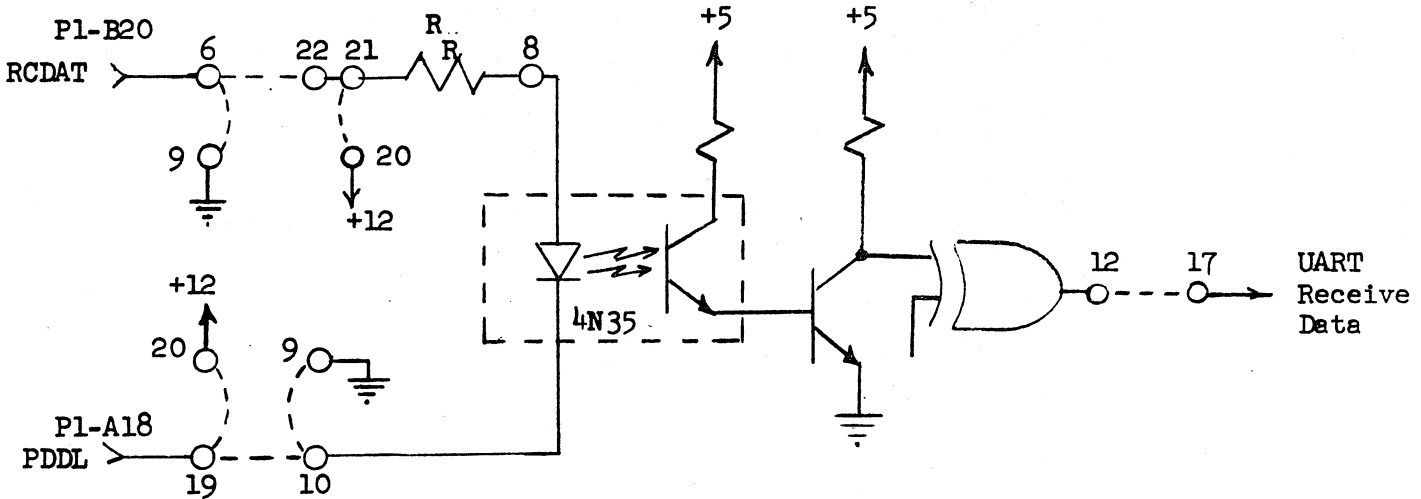


Figure A.10 Current Loop Receive Jumpers

The basic restrictions for the two circuits are concerned with the magnitude and polarity of the external loop supplies. The more positive level voltages for unipolar operation should be applied to connector pins A29 (transmit) and B20 (receive) to avoid incorrect biasing of the photo transistor and Q1 or the receive photo-diode. In a similar fashion, the more negative voltage of a unipolar loop is input to SIO connector pins B19 (transmit) and A18 (receive). Bipolar transmission requires the most negative loop supply voltage to be input on connector pin B29. The magnitude restrictions are associated with the maximum voltages and currents through the transmit transistors, Q1 and Q2, and the receive photo-diode portion of the 4N35 photo-isolator. Section V provides more detailed information but a summary of the device characteristics is as follows:

Transmit Transistor (1/2 2N2223)

ABSOLUTE MAXIMUM RATINGS

Collector-Emitter Volts	60 volts
Continuous Collector Current	500ma
Device Dissipation @ 25°C Free Air Temp (Derate linearly to 200°C at 2.86 mW <sup>o</sup> /C per each half of 2N2222)	0.5watt

OTHER SPECIFICATIONS

V <sub>CE</sub> (sat) @ I <sub>B</sub> = 5ma, I <sub>c</sub> = 50ma	1.2 volts maximum
---	-------------------

Receive Photo-diode Portion of 4N35

ABSOLUTE MAXIMUM RATINGS

Continuous Forward Current	60ma
Reverse Voltage	6 volt
Power Dissipation @ 25°C Free Air (Derate 1.33mW/ <sup>o</sup> C above 25°C)	100mwatt

OTHER RATINGS

Minimum Current Transfer Ratio	40%
Maximum Forward Voltage Drop @ 10ma forward current	1.7 volts

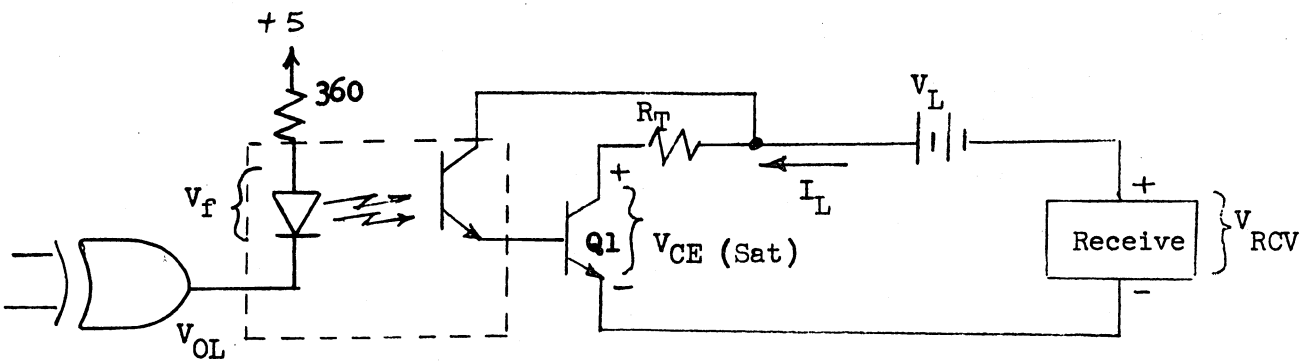
The 2N2223 limitation is primarily power dissipation; however, as can be seen from the  $V_{CE} (sat)$  figure, even at 50ma of collector current the device only drops 1.2 volts and dissipates only 60 mwatts. The photo-diode is limited by the input current which must be less than 60ma.

A.2.2.5 Limiting Resistor Calculations

$R_T$  and  $R_R$ , the current limiting resistors for unipolar loop operation, maintain currents within design limits to protect the SIO as well as the external loop circuits. For the case where the SIO provides the loop supply with the internal +12 volts, these resistors should be 510 ohms for 20ma loops over nominal distances where the line resistances are low. For long lines or when the line external voltages are different from +12 volts the values for limiting resistors may to be changed. Although the following discussions refer to the  $R_T$  and  $R_R$  resistors on the module, for long loops with relatively large line resistances the limiting resistance calculation includes the line resistance and this must be subtracted to give the module resistor values.

$R_T$  Value

A simplified transmit circuit for an externally supplied loop voltage looks as follows:



The photo-diode biasing is set up to provide approximately 10ma which even with a 40% current transfer ratio will allow the photo-transistor to supply 4 or more ma to the Q1. This is more than sufficient to turn Q1 on. Assuming a 20ma loop,

$$R_T = \frac{V_L - V_{CE(sat)} - V_{RCV}}{I_L} \quad V_{CE(sat)} \text{ for the 2N2222 is 1.2V max at 50ma}$$

20

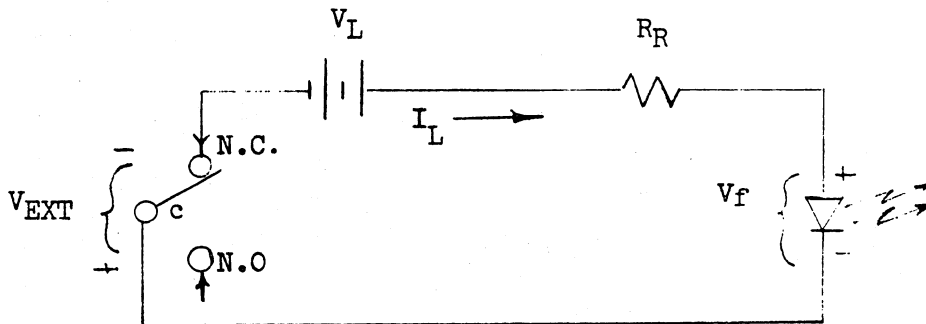
but will be less at 20ma. If the receive circuit is a photo-diode like that in the SIO,  $V_{RCV} = V_f$  which varies from 1.15 to 1.25 volts with 10 to 40ma forward current. Assuming values of 0.5v for  $V_{CE(sat)}$  and 1.2v for  $V_f$ ,  $R_T = \frac{V_L - (0.5) - 1.2}{I_L}$ . For a loop supply voltage of 12 volts

$$R_T \approx \frac{10.3}{20\text{ma}} \approx 515 \text{ ohms. Use 510 ohms for } R_T.$$

Note that  $R_T$  is the total loop resistance and includes line resistance and could also include an external current-limiting resistor in the remote device. It is possible that no resistance would be needed in which case a jumper would be used on the module between pins 2 and 27.

### R<sub>R</sub> Value

The receive circuit for an externally supplied loop voltage looks like the following:



$R_R = \frac{V_L - V_{EXT} - V_f}{I_L}$ . The major restriction is the absolute maximum continuous  $I_L \leq 60\text{ma}$ . As noted in the  $R_T$  calculations,  $V_f$  is 1.15 to 1.25 for 10 to 40ma loop currents. Again if we assume a 20ma current loop with a  $V_{ext} = .5\text{V}$ , an approximation is  $R_R \approx \frac{V_L - 1.7}{20} \text{ K}$ . As before with  $V_L = 12\text{V}$ ,  $R_R = 515 \text{ ohm}$  or 510 ohm using standard values. As in the case of the  $R_T$  calculations, it is possible to have a current limiting resistor in the external circuit. In this case the  $R_R$  above should be the total of both limiting resistors. In some cases, it may not be necessary to have a limiting resistor in series with the SIO photo-diode.

### A.3 Jumper Module Configurations

The following seven figures show the jumper module as it should be wired for RS-232-C (Figure A.11.a) and six (Figures A.11.b to A.11.g) current loop variations. The jumpers are shown as dashed lines.

Figure A.11.a-RS232C

Figure A.11.b-Current Loop, Separate Loops-Externally powered loops

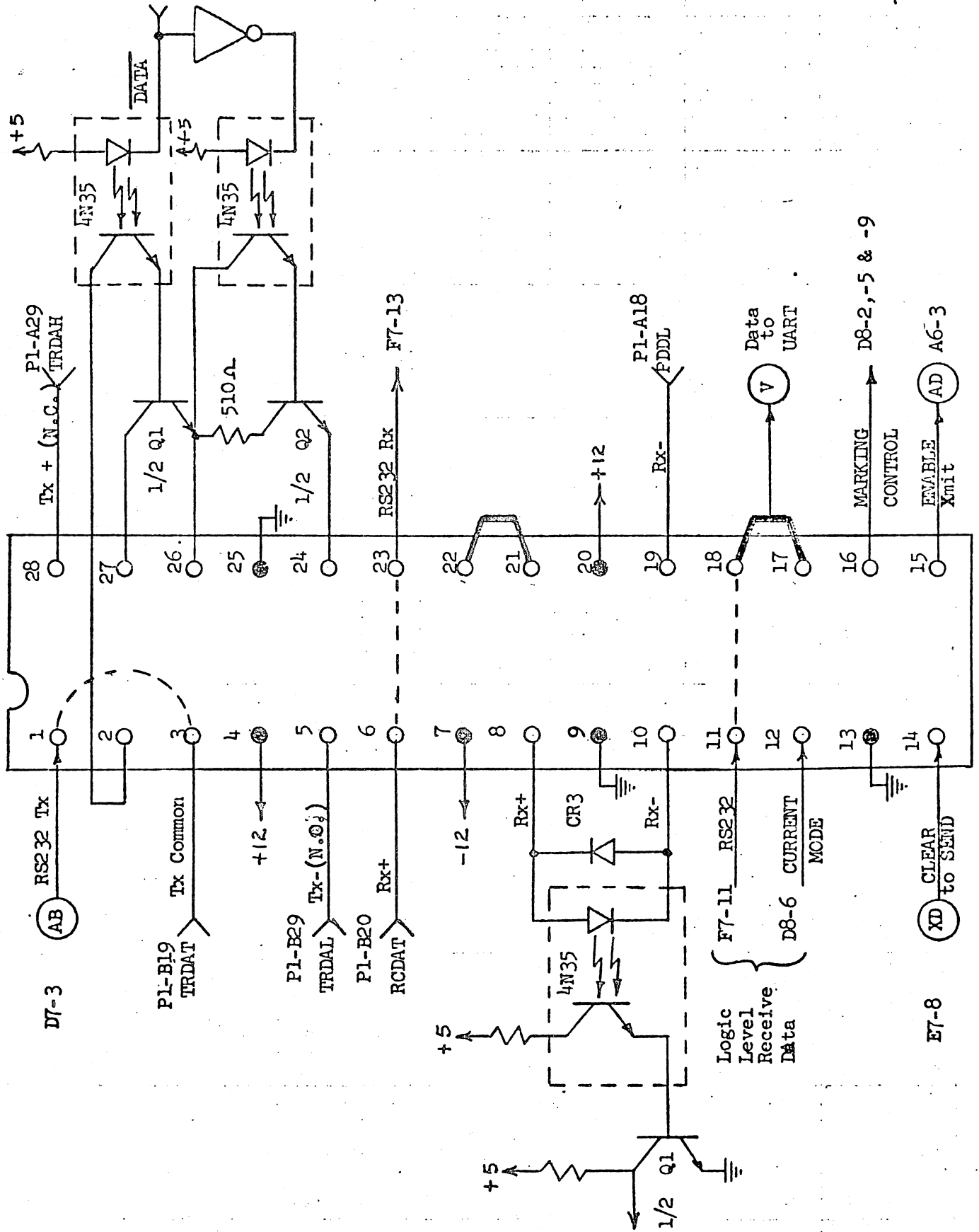
Figure A.11.c-Current Loop, Separate Loops-SIO powered loops

Figure A.11.d-Current Loop, Separate Loops-SIO powers transmit, externally powered receive

Figure A.11.e-Current Loop, Separate Loops-SIO powers receive, externally powered transmit

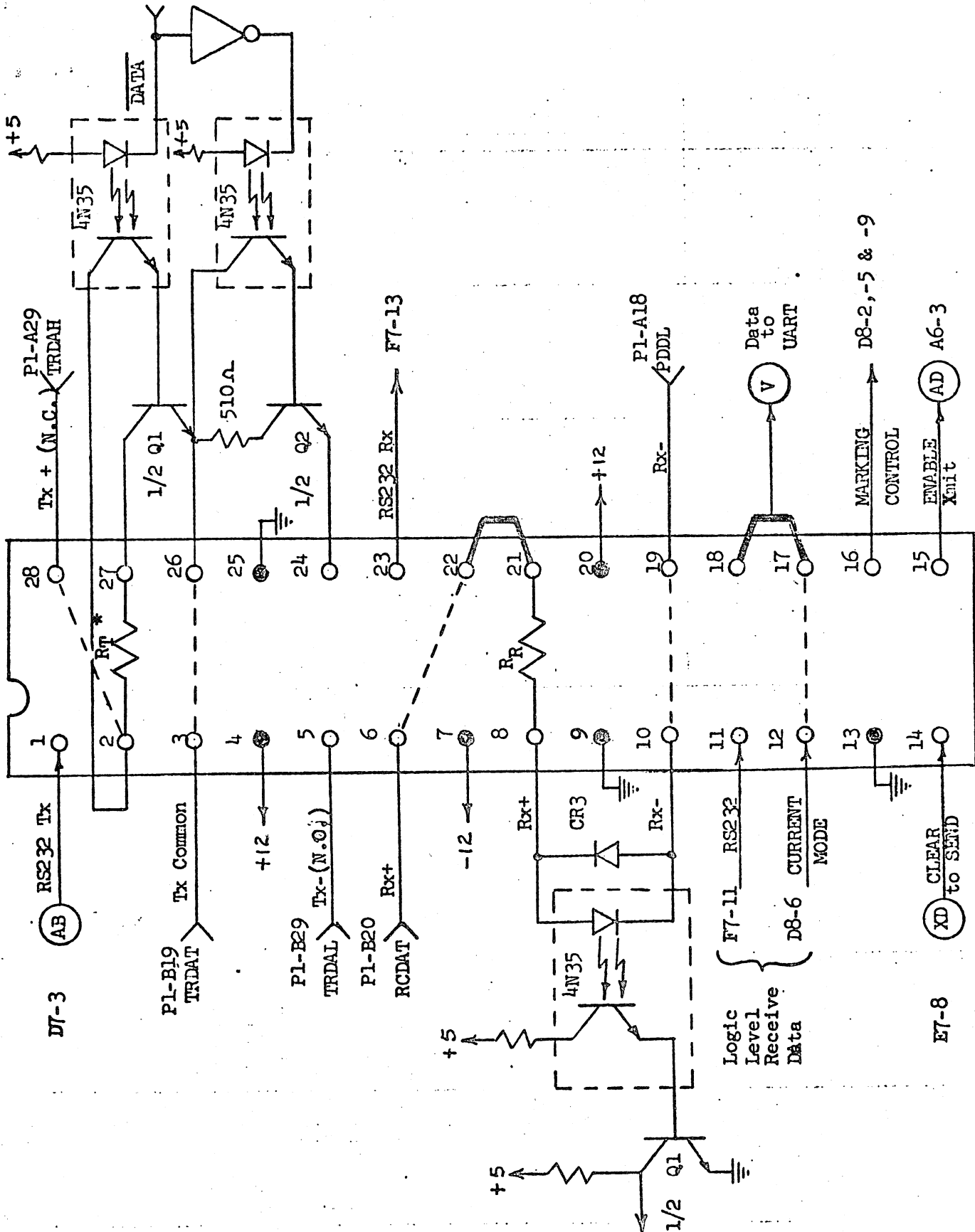
Figure A.11.f-Current Loop, Common Positive-SIO powered loops

Figure A.11.g-Current Loop, Common Negative-SIO powered loops



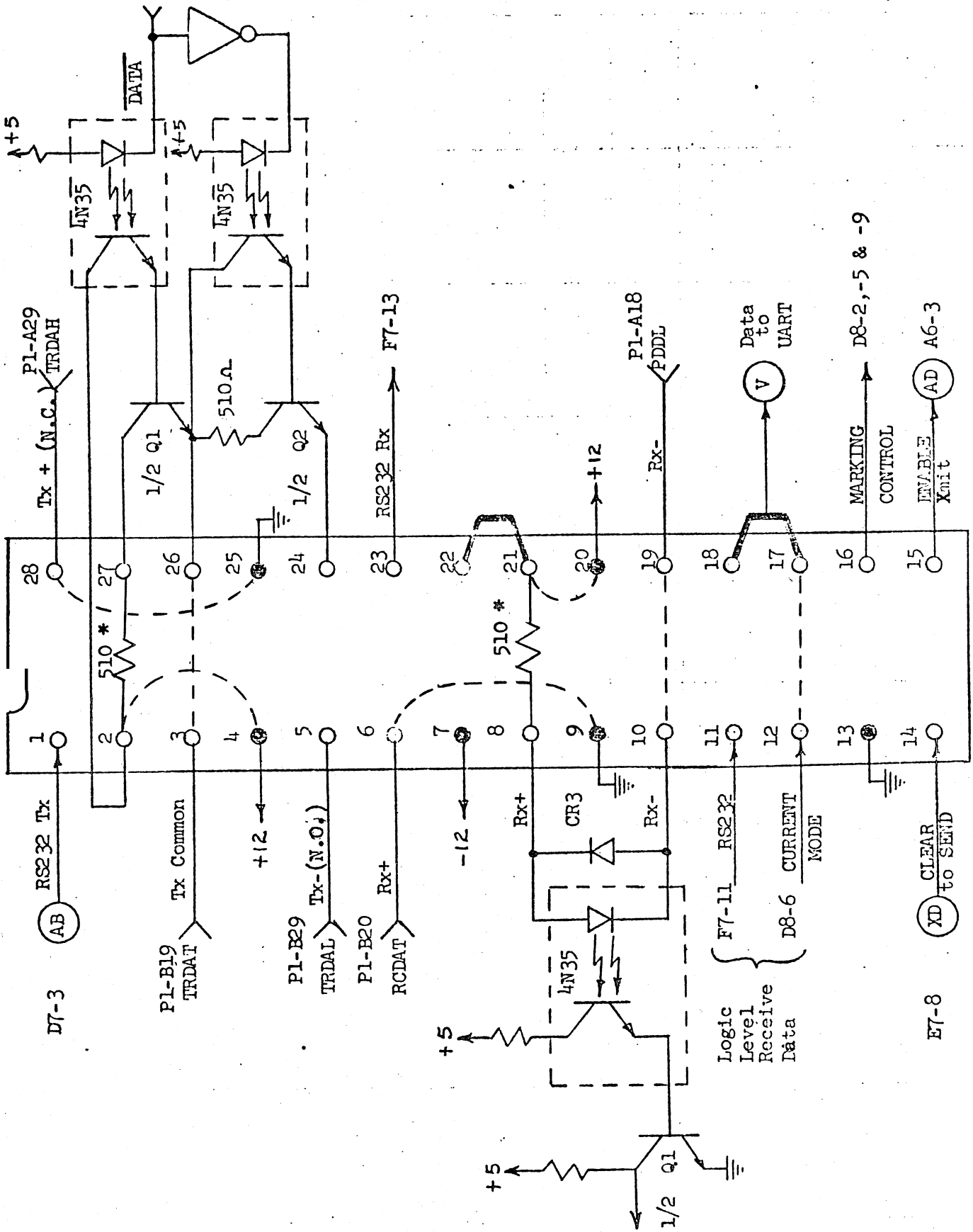
● GROUND, +12 TIE POINTS

Figure A.11a - RS 232-C



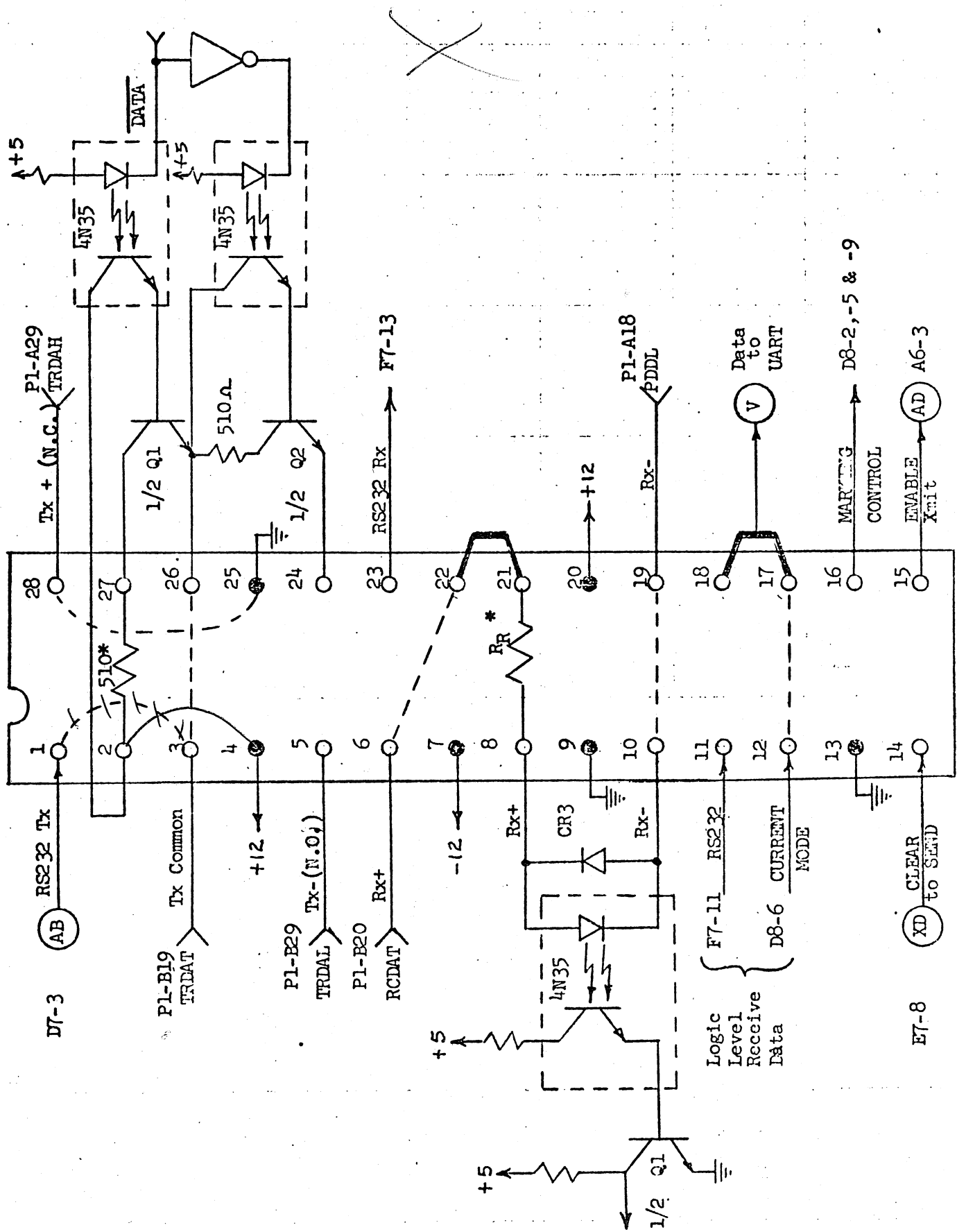
⊙ GROUND, +12 TIE POINTS \* See A.2.2.5

Figure A.11b - Current Loop, Separate Loops - External Loop Supplies



⊙ GROUND, +12 TIE POINTS \*Nominal - See A.2.2.5

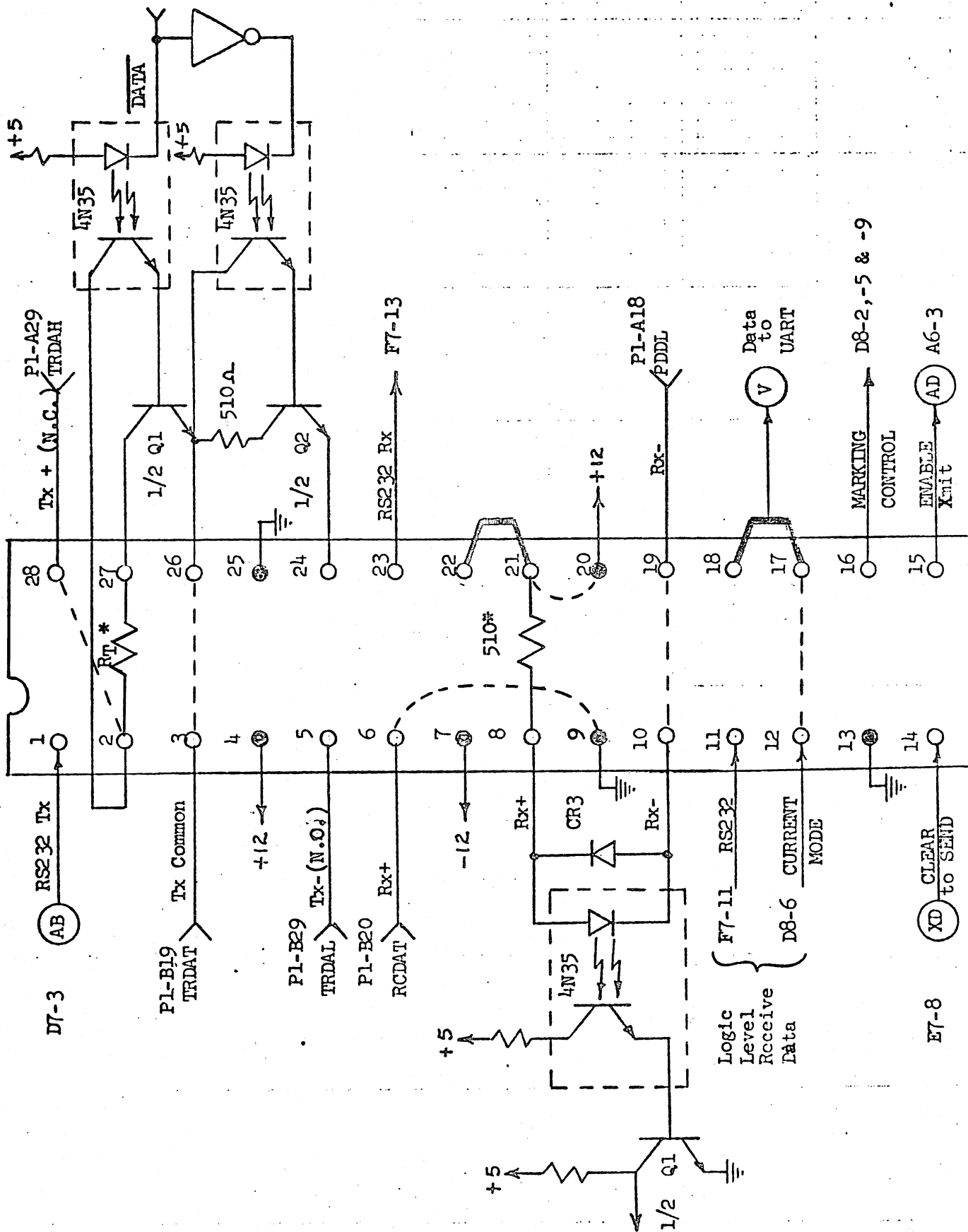
Figure A.11c - Current Loop, Separate Loops - SIO Supplies Power



⊕ GROUND, ⊖12 TIE POINTS

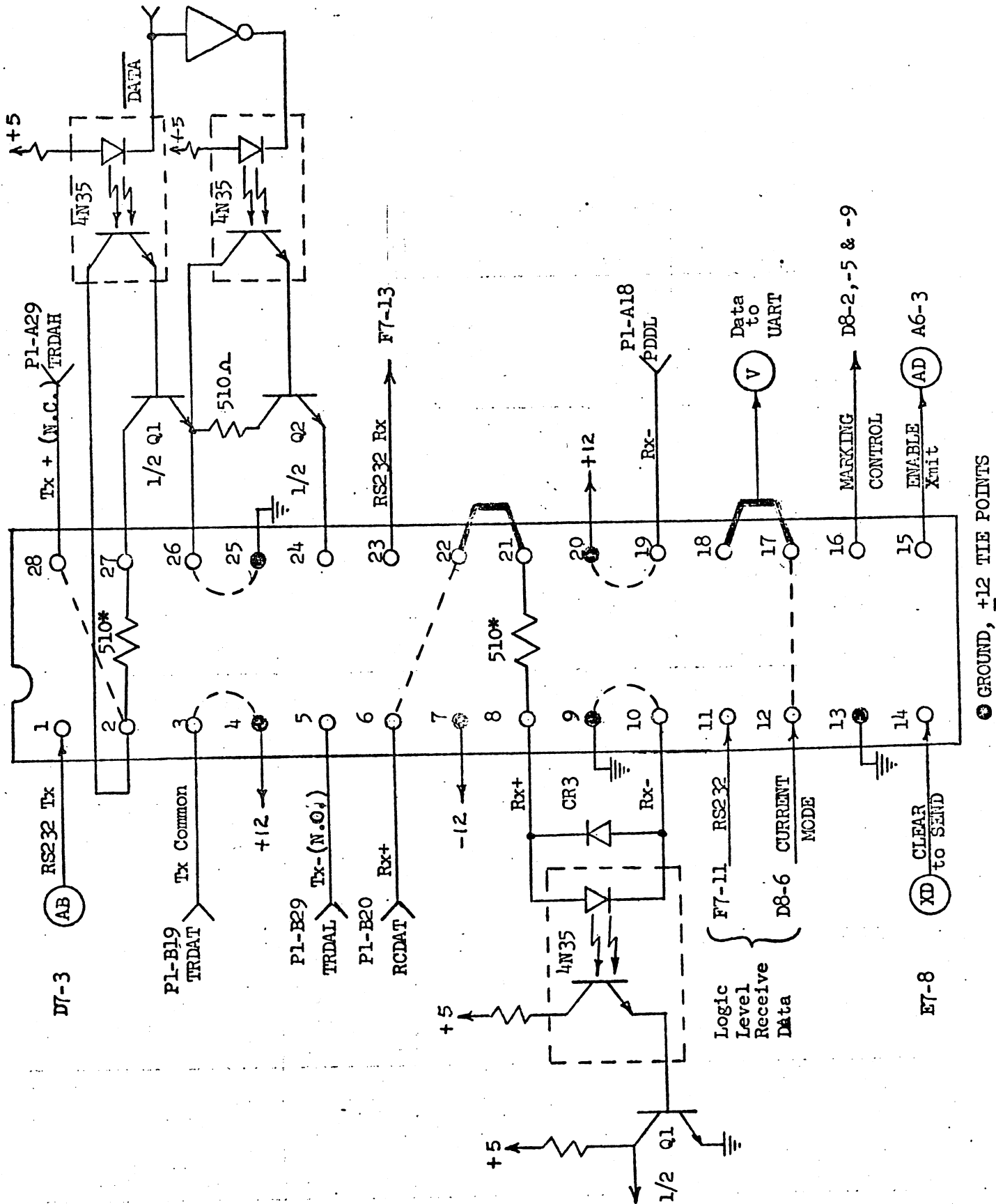
\* See A.2.2.5

Figure A.11d - Current Loop, Separate Loops - SIO Powers Send, Externally Powered Receive



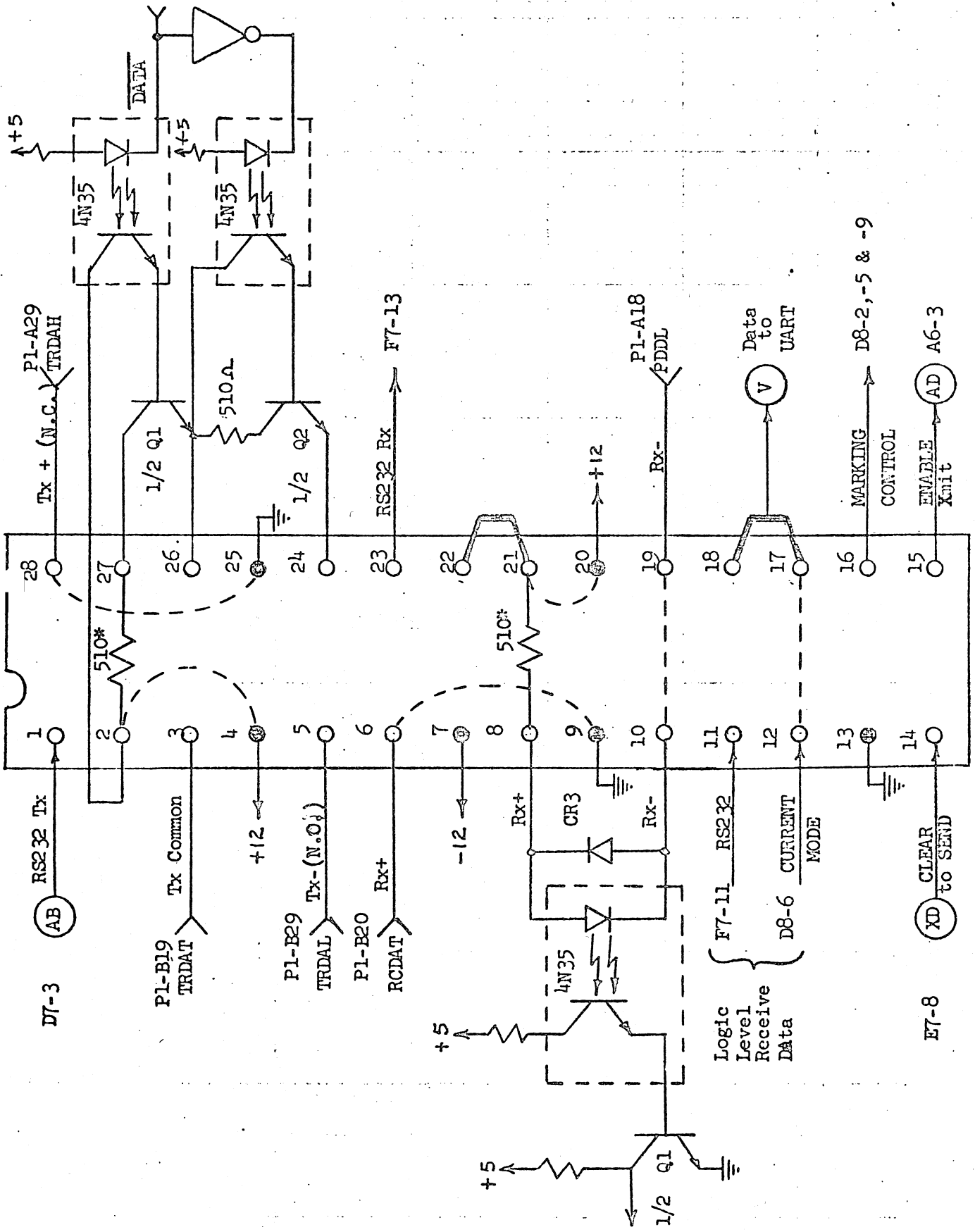
\*See A.2.2.5

Figure A.11e - Current Loop, Separate Loops - SIO Powers Receive, Externally Powered Send



\*Nominal - See A.2.2.5

Figure A.11f - Current Loop, Common Positive SIO Powered Loops



⊗ GROUND, +12 TIE POINTS

\*Nominal - See A.2.2.5

Figure A.11g - Current Loop, Common Negative - SIO Powered Loops

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